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A Survey on Architectures of MAC units for DSP Applications

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ABSTRACT

In today's smart and digital world, the brisk encroachment in science and technology has boosted up the requirements for Digital Signal Processors (DSPs) which are having superior computing efficiency, high speed and low power consumption along with real time application feasibility. For designing any Digital Signal Processors or other applications related to signal processing, Multiply-Accumulate (MAC) unit is one of the most vital blocks of processor. The performance of the designed MAC unit in turn evaluates the eventual whole and sole performance of any system of application. Hence, the speed, power consumption, area etc. have been the key spots of apprehension in progression of a variety of MAC architectures. This paper facilitates a generic survey on various techniques utilized to implement MAC units to enhance the performance. The presented survey paper finally promotes the researches to implement an efficient MAC architecture for applications related to digital signal processing domain.

Key words: Digital Arithmetic, Multiply-Accumulate (MAC) Unit, On-Silicon Area, Power Consumption, Mean Square Error (MSE).

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1. INTRODUCTION

Multiplication and accumulation are basic and significant operations occurring in all microprocessors, microcontrollers, digital signal processors and other data computing units. The Multiply Accumulate (MAC) units are having variety of applications in convolution, correlation, data and image processing, signal processing and filter designs etc. Hence, performance of these MAC units determines the performance parameters such as delay, area, and power consumption etc. of the digital processors. Hence, designing of optimized MAC units is one of the most promising areas of research nowadays. The generic architecture of MAC units consists of multiplier, adder and accumulator register. The multiplier performs the generation of partial product, reduction of generated partial product, propagation of carry and addition of propagated carry. Moreover, the accumulator is a general PIPO (Parallel Input Parallel Output) shift register. This performs the storage of the result generated after data accumulation. The current result obtained from multiplier is further added with the previous stored result of accumulator in adder unit.

Designing of low power and high speed MAC units is one of the prime and most demanding for real time digital signal processing based applications such Machine learning, Artificial Intelligence, Bio-medical signal processing, Audio and video signal processing, RADAR and other defense related applications [1-5]. Furthermore, the analog signal processing schemes are employed in digital domain with the extensive usage of a variety of signal processing techniques such as Fast Fourier Transform (FFT), Discrete Fourier Transform (DFT), Z-Transform etc. in order to reduced the circuit complexities, power consumption, execution and computation time.

Number of researches is going on in order to design the multiplier and adder units with less delay, high speed, and low power consumption along with compacted chip level implementation [6]. In any DSP processor, the overall performance and its execution time mainly depends on multiplier and adder units only. The usage of repeated bit addition and bit shifting operations make multiplication of binary numbers more efficient and optimized. However, usage of generic adders creates an overhead in terms of delays due to carry generation wait time. Hence, the multipliers using such adders consume more power and are quite slower [7]. These constraints make inroads to research for designing efficient adders and hence multipliers using optimized adders.

The rest of the paper is planned as follows. Section 2 presents the literature survey which covers different design architectures of MAC units. Section 3 presents comparison of different MAC units discussed in section 2 based on different performance parameters. Section 4 presents the conclusion of the paper.

2. LITERATURE SURVEY

This literature survey talks over a variety of approaches aiming towards the enhancement in the performance of adders, multipliers and hence multiply accumulate (MAC) unit. VLSI based design and implementation of the adder, multiplier and MAC circuit for digital signal processing applications is one of the most challenging tasks. Since, Moore's law depicted that the number of transistors on a silicon chip unit area would get double in every eighteen months. As a result, the area of the chip gets reduced. However, the key challenging issues are delay, power consumption and area. In order to resolve these issues, lots of researches have been evolved. In this section author will discuss few methodologies which will help to open a scope for further research.

Design of a floating point multiply and accumulate unit was done using old mathematics in [8] which results in the reduction of the number of partial products which are going to be added. This results in enhancement of speed of accumulation of generated partial products from multipliers. This is mainly due to reduction in number of stages occurring in generation of partial products which are ready to be added. This results in a design of MAC unit which is having superior performance. As compared to the existing conventional mathematical techniques, the implemented scheme is better in terms of computation and speed. Hence, this implementation is tremendously advantageous for digital signal processing applications.

A new scheme was proposed in order to design both signed and unsigned fixed-width multipliers with minimal mean square error (MSE) in [9]. This novel methodology results in improvement of power dissipation, on silicon area, results accuracy and timing performances as compared to the existing schemes. The design was implemented in 180nm technology. Results obtained with proposed implementation show the reduction in power dissipation by 50% and 13% decrease in propagation delay. An area and Delay efficient design of MAC unit was proposed with the extensive use of adapted Low Area Wallace tree multiplier (LAW) in [10]. The proposed multiplier was useful in order to design high speed applications of digital signal processing field.

Different methodologies in order to design the MAC unit were discussed in [11]. The comparison of discussed schemes was done for analysis of performance based on the various performance parameters such as power consumption, speed, delay and area. However, the 8 bit MAC based on Baugh-Wooley Multiplier was having extremely low power consumption but at the cost of increased delay and with respect to the other schemes. Furthermore, the 32 bit MAC based on Baugh-Wooley with HPM reduction results in lesser silicon area lower, power dissipation and equivalent delay as compared to the modified Booth multiplier. The power consumption can further be reduced with extensive use of pipelining.

Design of variable-correction based truncated multipliers was proposed in [12]. In this scheme, few of the generated partial-products are treated as redundant and are discarded in order to reduce the design complexity. Furthermore an appropriate compensation function was further added in order to compensate the introduced error to some extent. However, the optimal compensation function in order to minimize the mean square error was also designed in this work. An implementation of MAC unit based on reversible logic gates which is essential for quantum computers was done in [13]. A novel circuit of 4x4 bit reversible logic based multiplier was designed using Peres gates and HNG gates. The proposed reversible multiplier circuit was found to be better as compared to existing designs in terms of gate count, quantum cost and hardware complexity. An efficient numerical scheme in order to calculate the maximum absolute error (MAE) in fixed-width multipliers and hence fixed-width multiplier-accumulator (MAC) circuits was implemented in [14]. In addition to this, a compensation function was also evaluated in order to minimize this maximum absolute error (MAE) and was implemented efficiently in hardware too. Some other design of efficient MAC units based on lower error fixed width multiplier [15], Baugh-Wooley multiplier [16], 2-Cycle Multiply-Accumulate architecture [17], decimal floating-point fused concept based [18] etc. were also proposed.

3. COMPARISON OF DIFFERENT COMPRESSION SCHEMES

Table-1 presents a comparative analysis of various compression schemes discussed and surveyed in this paper. The different compression techniques along with their pros and cons are listed in this table. They are arranged in sequence of reference citation order in this table. The selection of particular compression scheme depends on the choice of performance parameters such as on silicon area, speed, power consumption, timing delay, circuit complexity along with implementation and application domains.

Table -1 Comparison of Different Mac Units

MAC Architecture	Advantages	Disadvantages	Applications
Meenu S Ravi et. al [8]	Good Speed Superior Computation Moderated power consumption	Complex Circuitry Moderated Area	Digital Signal Processing Filter Design
N. Petra et. al [9]	Superior MSE Superior Computation	More Area More Delay	Fixed Width Multiplier for

		More Power Consumption	Numerical Computations
G.Indira et. al [10]	Less Area High Speed	More Power Consumption	Digital Signal Processing Filter Design
Ku. Shweta et. al [11]	Low power consumption Less Area	Extremely Large Delay	FFT, DCT computations
N.Petra et. al [12]	Superior MSE Superior Computation Less Delay	More Area More Power Consumption	Digital Signal Processing FIR Filter Design
Shaik Nasar et. al [13]	Less Delay Less Gate Count Less Area	More Quantum cost More Power	Digital Application and ALU units
Davide De Caro et. al [14]	Superior MSE Superior Computation Less Delay Low power consumption	More Area	Digital Signal Processing FIR Filter Design
Tung Thanh Hoang et. al [17]	Low power consumption Moderated Delay	More Area	ALU Units

4. CONCLUSION

This paper has presented a widespread and up to date survey on various designs and architectures of adders and multipliers and hence Multiply-Accumulator (MAC) units. Since, speed and power consumption are one of the most challenging issue during the designing of MAC units and especially in case their usages in the domain of digital signal processing and multi-rate filter designing. Moreover, the on silicon area is also equally noteworthy in order to design an efficient and prolific MAC unit in order to perform arithmetic in multi-rate filters. In order to evolve an efficient VLSI design of MAC unit, different performance metrics are equally important upon which the discussion has been already conducted in respective sections. The summarized table is also presented in section 3 considering all the various MAC architectures aiding their pros and cons along with their applications.

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