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European Journal of Advances in Engineering and Technology, 2019, 6(10):7-20

Research Article ISSN: 2394 - 658X

Grid Voltage Profile Enhancement using UPFC based on Harmony Search Algorithm

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ABSTRACT

In this paper, a dynamic model of Unified Power Flow Controller (UPFC) is developed to improve the power transfer capability (PTC) through the transmission line. Improvement of the buses voltage profiles along with the reduction of total power losses is also intended with UPFC's presence. The UPFC shunt and series controllers are developed based on two types of controllers Fuzzy Logic Controller (FLC) and PI Controller which has been planned in Matlab Simulink software. The gains values are optimized using Harmony Search Algorithm. Sinusoidal pulse width modulation (SPWM) technique is applied as a modulation technique to generate switching signals for the converter switches. The proposed UPFC controller is tested by using IEEE-15 bus radial system with different case studies.

Key words: Unified Power Flow Controller (UPFC), Harmony Search Algorithm (HS), Power flow Control, Fuzzy Logic Controller (FLC).

1. INTRODUCTION

1.1. Load compensation, voltage balancing and voltage regulation are some of the main problems which may be happened in the grid and cause power losses in lines, mal-operation of critical loads, damage to customer equipment, and potentially power system instability. Reactive power compensation is typically required to solve the above problems. Reactive power compensation devices are called (FACTS).

1.2. Flexible AC Transmission System (FACTS) is one aspect of power electronics revolution that is taking place in all areas of electric energy. FACTS controllers use multiple power electronic circuits or equipment that perform certain function like current control, power control, etc., and can be used in generation, transmission and distribution of electric energy.

1.3. The static series synchronous compensator (SSSC), static synchronous compensator (STATCOM) and Unified Power Flow Controller (UPFC) are the main types of Flexible AC Transmission System (FACTS).

1.4. The static series synchronous compensator (SSSC) can control active and reactive in a transmission line in a small range via storied energy in capacitor DC-link where static synchronous compensator (STATCOM) with injecting reactive power can maintain the bus voltage in a transmission line. Unified Power Flow Controller (UPFC) is the most multilateral and complex Flexible AC Transmission Systems (FACTS) equipment that has emerged for the control and optimization of power flow in power transmission systems [1-3]. It has the combining features of both series converter and shunt converter based FACTS devices, and is capable of inquiring voltage regulation, series compensation, and phase angle regulation at the same time. Therefore, the UPFC is capable of independently controlling the active power and reactive power on the compensated transmission line [4, 5]. The electric utilities are continuously looking for new devices that will enable interconnected systems to have increased power transfer abilities with transmission lines.

1.5. The unified power flow controller consists of two voltage source Converters (VSCs) that are connected to a common DC- link. One of the VSCs is connected in series with a transmission line while the other one is connected in shunt with the same transmission line. The DC bus of both VSCs are supplied through a common DC capacitor, hence UPFC combines the functions of a STATCOM and a SSSC. STATCOM maintains constant the bus voltage and provide energy for DC link of SSSC and it can regulate capacitor's voltage of DC link, SSSC with injection controllable voltage controls the active and reactive power flow control in the transmission line [6].

1.6. Two Types of controller based UPFC has been designed to control the active and reactive powers flow in transmission line. Proportional and integral (PI) Controller. Also, Fuzzy Logic Controller (FLC) are employed to develop the control algorithms for both shunt and series converters of UPFC. The
advantages of FLC over other controllers are it doesn't need an accurate mathematical model of the system and it is robust to power system parameters changes and dynamic operations. IEEE-15 bus radial system is considered as a case study. The performance of the proposed controller based UPFC has been designed in Matlab Simulink software and applied on the system at three different operating conditions of the power system network. Under Over Loading operating condition, under variable loading operation and during three phase short circuit fault are the three different operating conditions.
The gains for both controller (PI &FLC) have been determined using Harmony Search Algorithm optimization control technique.

2. TEST SYSTEM MODEL

IEEE-15 Bus Radial system is the electrical network which will be used to analyze the performance of the proposed controller. IEEE-15 Bus network is shown in figure.9 .it is operating at nominal voltage 11K Volt. With two generation bus. one is Synchronous generator at bus No.1 (Swing bus) with rating 3 MVA and the other is Diesel Generator with rating 300 KVA at bus No.3 (PV bus). The Network parameters are shown in table 1 & 2. The location of UPFC in IEEE-15 bus network has been chosen at line 4-5 using try and error method.

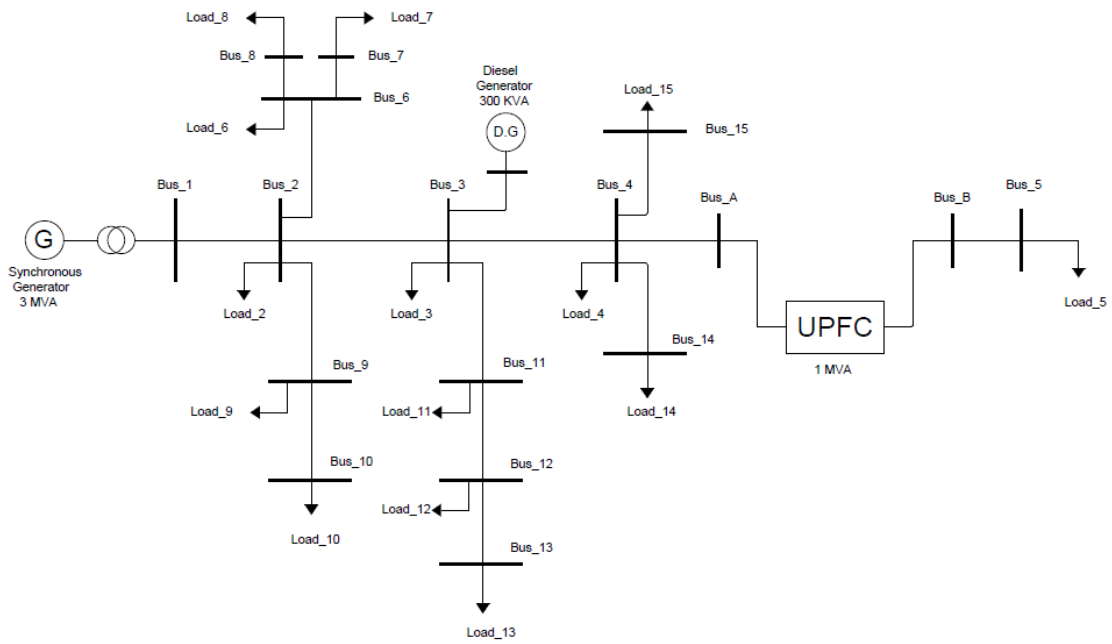


Fig. 1 Single line diagram of IEEE 15 bus radial system

2.1. IEEE-15 Bus Radial System Parameters

Table-1 Transmission Line Data - IEEE 15 Bus radial system

Line Impedance				
	From Bus No.	**To Bus No.**	**Resistance(ohm)**	**Reactance(ohm)**
Line 1	1	2	1.35309	1.3235
Line 2	2	3	1.17024	1.144658
Line 3	2	6	2.55727	1.724885
Line 4	2	9	2.01317	1.357884
Line 5	3	4	0.8411	0.8227
Line 6	3	11	1.79553	1.00923
Line 7	4	5	1.53248	1.0276
Line 8	4	14	2.23081	1.50468
Line 9	4	15	1.19702	0.8074
Line 10	6	7	1.0882	0.734
Line 11	6	8	1.25143	0.844083
Line 12	9	10	1.68671	1.13768
Line 13	11	12	2.44845	1.6513
Line 14	12	13	2.01317	0.0036019

Table-2 Bus Data - IEEE 15 Bus radial system

Bus Data						
Bus No.	**Voltage Magnitude(P.U)**	**Angle in Degree**	**Generation Bus**		**Load Bus**	
			Q (K VAR)	**P (K WATT)**	**Q (k VAR)**	**P (k WATT)**
1	1.02	0	984.745	964.392	-	-
2	0.999	0.03	-	-	44.9	44.099
3	0.991	0.04	300	300	71.41	70
4	0.985	0.05	-	-	142.82	140
5	0.984	0.06	-	-	44.99	44.1
6	0.986	0.17	-	-	142.82	140
7	0.985	0.19	-	-	71.4	70
8	0.984	0.2	-	-	142.82	140
9	0.996	0.06	-	-	71.4	70
10	0.995	0.08	-	-	44.99	44.1
11	0.984	0.12	-	-	71.41	70
12	0.978	0.19	-	-	44.99	44.1
13	0.974	0.24	-	-	142.82	140
14	0.981	0.1	-	-	142.82	140
15	0.984	0.06	-	-	71.4	70

3. UPFC MODEL

A dynamic model of the UPFC is shown in Fig. 1. UPFC connects to the transmission line with shunt and series voltage source converters (VSC) which are coupled via a common DC link. Normally, the shunt VSC is considered as (STATCOM) and series one as a static compensator (SSSC). Low pass AC filters are connected in each phase to prevent the flow of harmonic cur-rents generated due to switching. The transformer connected at the output of converters to pro-vide the isolation, modify voltage/current levels and also to prevent DC capacitor being shorted due to the operation of various switches. Insulated gate bipolar transistors (IGBTs) with anti-parallel diodes are used as switching devices for both converters [8].

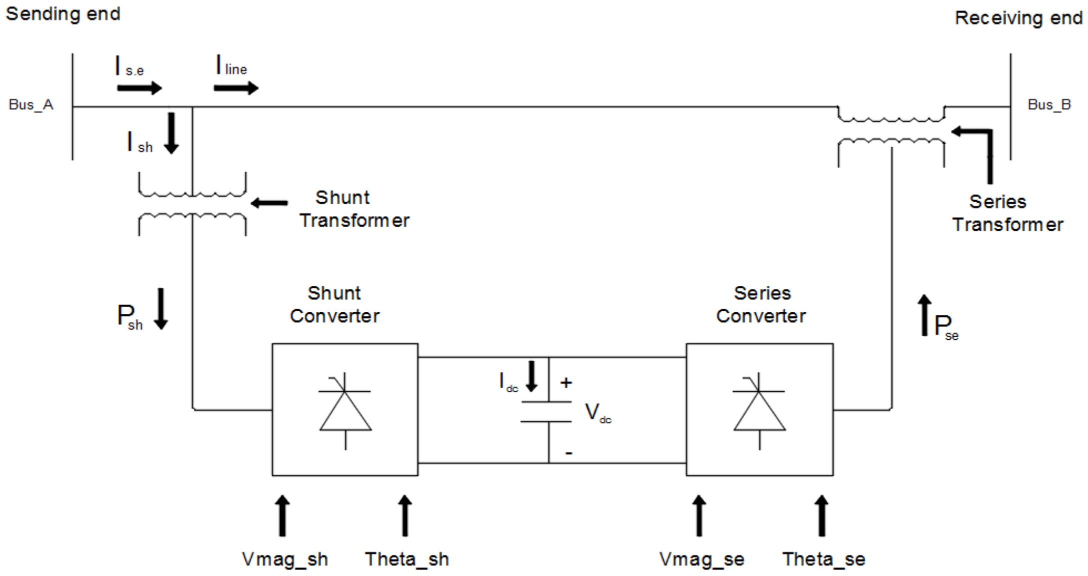


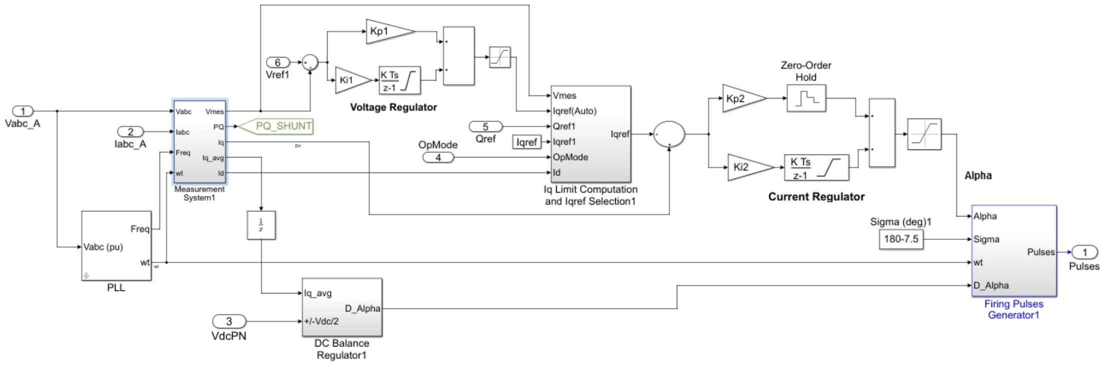
Fig. 1 UPFC Model

3.1 UPFC Controller

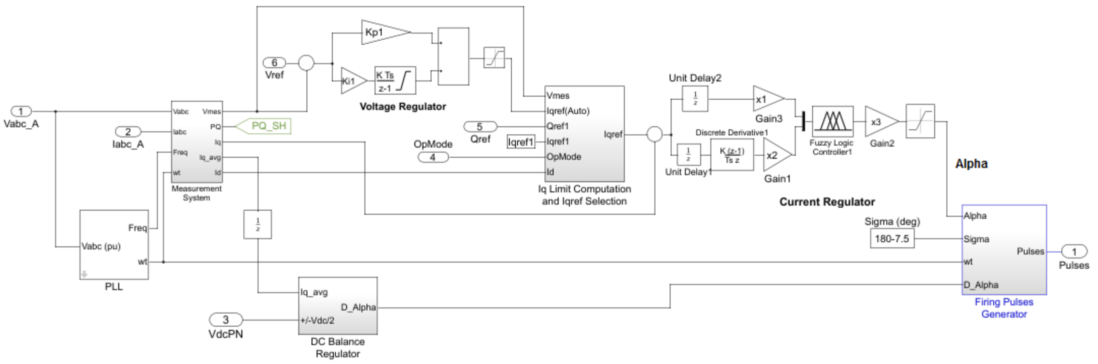
UPFC controller consists of shunt and series controllers for both shunt and series converters. To achieve real and reactive power flow control in transmission line, UPFC controller has been designed to control active and reactive power flow and magnitude of the series injected voltage.

3.2 Shunt Converter Controller

The control algorithm of shunt controller builds inside Matlab software is shown in Fig. 2 represents the controller of sending - end voltage and current to generate (Alpha) and SPWM technique to generate the firing signals for the UPFC shunt converter switches.



(a)



(b)

Fig. 2. (a) Matlab Simulink Shunt Converter Controller Based PI controller, (b) Matlab Simulink Shunt Converter Controller Based Fuzzy Logic controller

The shunt converter draws current from the sending - end of the transmission line to keep the voltage of the DC link capacitor at its reference value by drawing real power from the line and to maintain the sending - end voltage at its reference value by absorbing or providing reactive power to the transmission line. To simplify the dynamic analysis we have a measurement system block at where three phase shunt current at Bus No. A (Ia_sh, Ib_sh and Ic_sh) have been converted to d-axis and q-axis components in a synchronously rotating d-q frame (Idsh_measured and Iqsh_measured). Also three phase shunt voltage at Bus No. A (Va sh, Vb_sh and Vc_sh) have been converted to d-axis and q-axis components in a synchronously rotating d-q frame (Vdsh_measured and Vqsh_measured) and Thus we can get at the magnitude (Vmag_sh) and phase angle (__sh) of the sending end voltage from the following equation:

$$Vmag\_sh = \sqrt{V^2{}_{d\_sh} + V^2{}_{q\_sh}} \quad (1)$$

$$\alpha\_sh = \tan^{-1} \frac{V_{q\_sh}}{V_{d\_sh}} \quad (2)$$

At voltage regulator controller, the magnitude value of sending end voltage has been compared with ref value and the error signal has been given as an input to controller block to control the sending – end bus voltage. The output of controller gives reference quadrature component (Iqsh_ref) of the shunt current (Ish). At current regulator controller. The measured value of the quadrature shunt current (Iqsh_measured) has been compared with obtained reference quadrature shunt current (Iqsh_ref) and the error signal has been given as inputs to controller block which generate an output signal [angle (_sh)] to pulse generator block.

To generate the switching firing signals, sinusoidal pulse width modulation (SPWM) has been used. For this purpose, the phase angle of the reference sine wave has obtained from the difference (angle_s −_sh) of the two angles where the angle (_sh) has been gotten from current regulator block and the angle (angle_s) is the sending-end voltage which has been extracted from phase locked loop (PLL). The magnitude (Vmag_sh) of the shunt sending end voltage obtained from equation (1) has been used as a magnitude for the reference sine wave. In the SPWM technique, the reference signals are compared with the carrier signal, to generate the switching firing signals (Q1_sh, Q2_sh, Q3_sh, and Q4_sh) for the shunt converter switches.

There are two types of controller will be used:

1- proportional and integral controller (PI CONTROLLER)

2-fuzzy logic controller (FLC)

NOTE: The Gains of PI controller and FLC will be determined by using <u>Harmony Search Algorithm.</u>

3.2.1 PI Controller

As shown in fig. 2(a) where there are two PI Controller one at voltage regulator controller and the other at current regulator controller and their gains are resulted from Harmony Search Algorithm which are shown at table-3.

Table-3 PI controller gains of UPFC shunt converter controller

Kp1	Ki1	Kp2	Ki2
0.3317	0.1522	0.348	0.1217

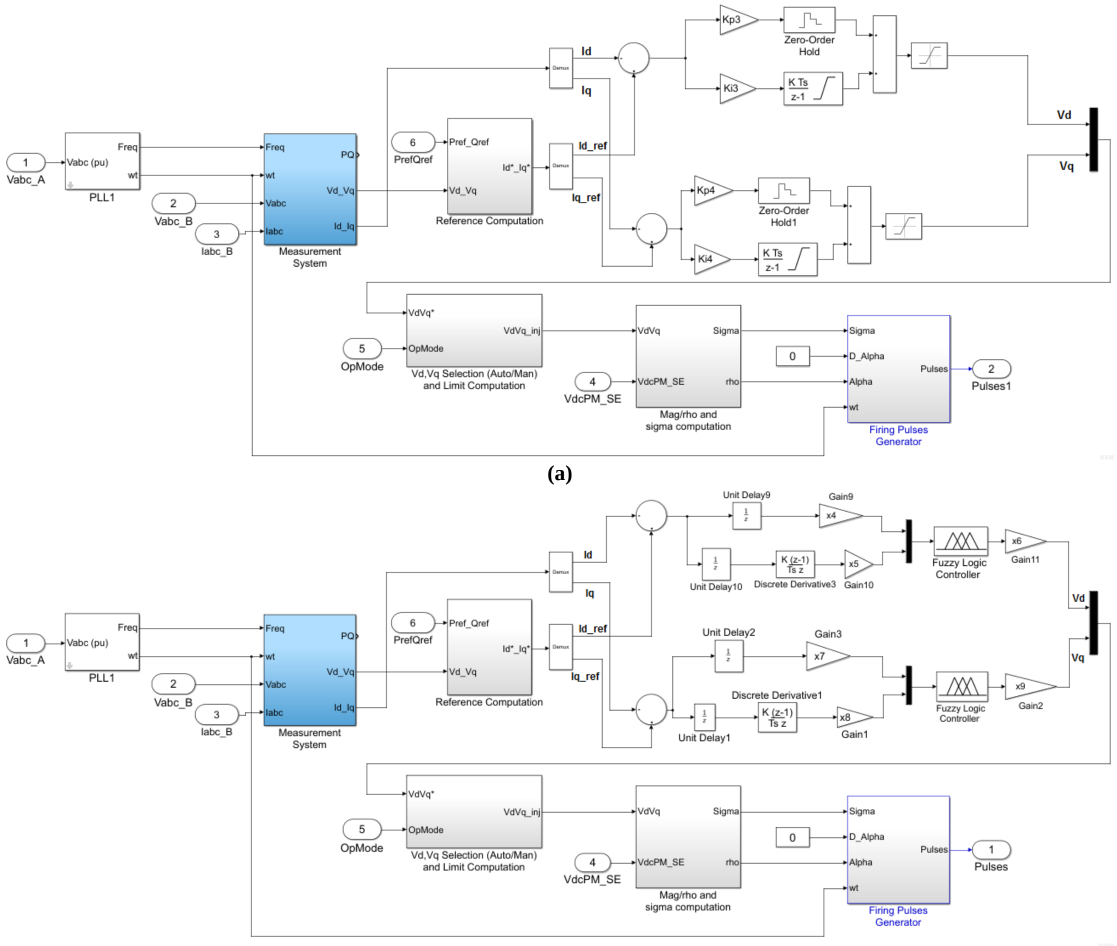
3.2.2 Fuzzy Logic Controller

As shown in fig. 2(b) where there are two Controller. One of them is PI Controller at voltage regulator controller and the other FLC at current regulator controller and their gains are resulted from Harmony Search Algorithm which are shown at table-4.

Table-4 PI controller & FLC gains of UPFC shunt converter controller

Kp1	Ki1	X1	X2	X3
0.72	0.15	0.4	70.2	82.5

3.3 Series Converter controller: The controller of series converter is illustrated in Fig. 3. The series converter controls the active and reactive power flow through the transmission line by injecting a voltage in series with the line current having controllable magnitude and angle.



(b)

Fig. 3 (a) Matlab Simulink Series Converter Controller Based PI controller, (b) Matlab Simulink Series Converter Controller Based Fuzzy Logic controller

To simplify the dynamic analysis we have a measurement system block at where three phase series current at Bus No. B (Ia_se, Ib_se and Ic_se) have been converted to d-axis and q-axis components in a synchronously rotating d-q frame (Idse_measured and Iqse_measured). Also three phase series voltage at Bus No. B (Va se, Vb_se and Vc_se) have been converted to d-axis and q-axis components in a synchronously rotating d-q frame (Vdse_measured and Vqse_measured).we can use Vd & Vq series signal to get at Id & Iq reference signal through reference computation block and (Id_se) has been compared with (Idse_ref) and the error signal is the input to the controller block to generate (Vd_se). Also, (Iq_se) has been compared with (Iqse_ref) and the error signal is the input to the controller block to generate (Vq_se) and thus, The outputs of the two controller provided the orthogonal components of the series injected voltage (Vq_se and Vd_se). The magnitude and phase angle of series injected voltage are obtained through the following equations:

$$Vmag\_se = \sqrt{V^2{}_{d\_se} + V^2{}_{q\_se}} \quad (3)$$

$$\alpha\_se = \tan^{-1}\frac{V_{q\_se}}{V_{d\_se}} \quad (4)$$

As like shunt converter controller in series controller also the process of switching signal generation has been conducted by using SPWM technique. The internal configuration of the SPWM technique used to generate switching signals for series converter switches. The magnitude of the reference sine wave has been obtained from equation (3) and the phase angle (Theta_se) is obtained by finding the difference (_r −_se) of receiving-end voltage angle (_r) obtained via PLL and angle (_se) obtained from equation (4). In SPWM, the reference sine waves are compared with carrier signal. The outputs of the SPWM have been provided as firing signals (Q1_se, Q2_se, Q3_se, andQ4_se) for the series converter switches.

Also, PI Controller and Fuzzy Logic Controller will be used in Series converter controller and their gains are optimized from Harmony Search Algorithm.

3.3.1 PI Controller

As shown in fig. 3(a) there are two PI Controller one at Id_se controller and the other at Iq_se controller and their gains are resulted from Harmony Search Algorithm which are shown at table-5.

Table-5 PI controller gains of UPFC series converter controller

Kp3	Ki3	Kp4	Ki4
0.8842	0.0943	0.93	0.399

3.3.2 Fuzzy Logic Controller

As shown in fig. 3(b) where there are two Controller. One of them is FLC at Id_se controller and the other FLC at Iq_se controller. Which their gains are resulted from Harmony Search Algorithm which are shown at table-6.

Table-6 PI controller & FLC gains of UPFC series converter controller

X4	X5	X6	X7	X8	X9
0.2	54.7	1.2	66.8	5.9	62.06

4. FUZZY LOGIC CONTROLLER PARAMETERS

Table-7 Rule table for Fuzzy Logic Controller

		Error-Rate						
		PL1	PM1	PS1	VS1	NS1	NM1	NL1
Error	PL	BP	BP	BP	MP	MP	SP	ZO
	PM	BP	BP	MP	MP	SP	ZO	SN
	PS	BP	MP	MP	SP	ZO	SN	MN
	VS	MP	MP	SP	ZO	SN	MN	MN
	NS	MP	SP	ZO	SN	MN	MN	BN
	NM	SP	ZO	SN	MN	MN	BN	BN
	NL	ZO	SN	MN	MN	BN	BN	BN

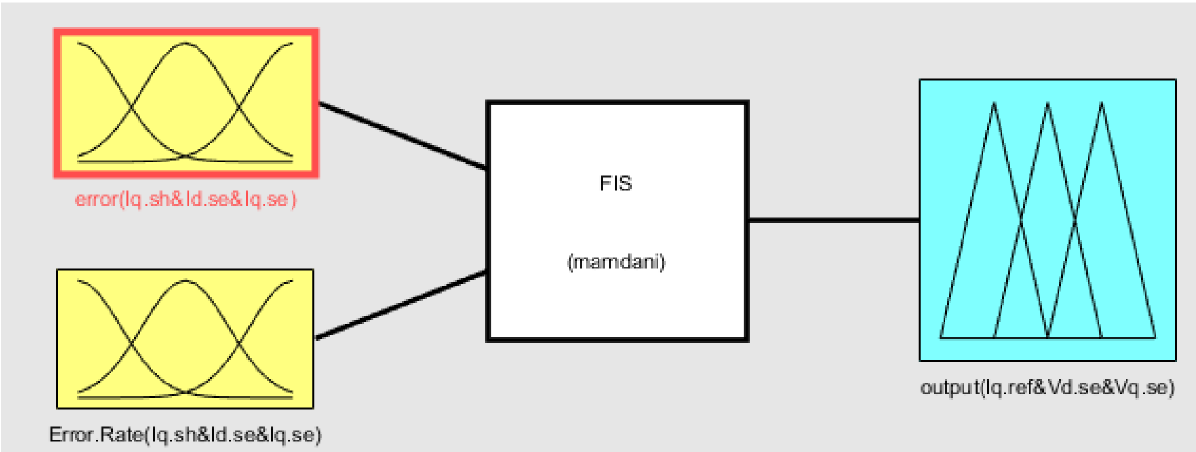


Fig. 4 Fuzzy Logic Controller Structure

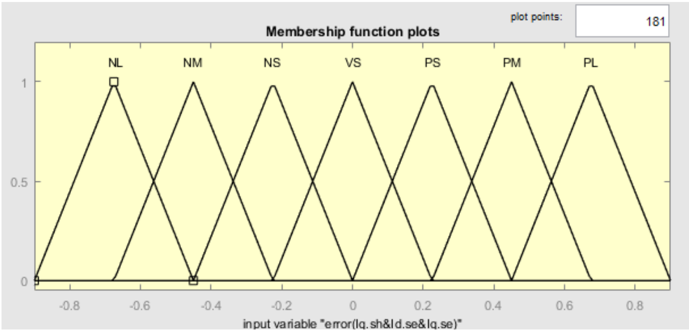


Fig. 5 Membership function of Error

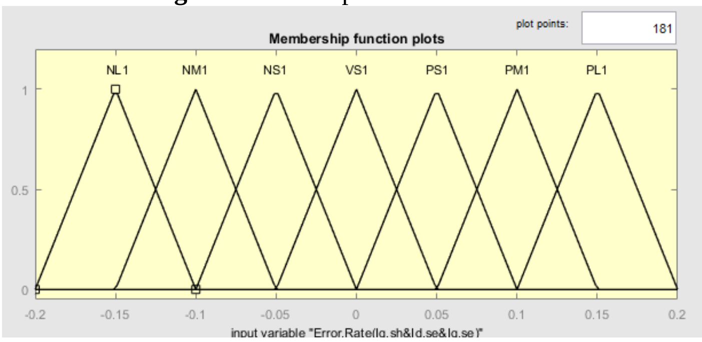


Fig. 6 Membership function of Error-rate

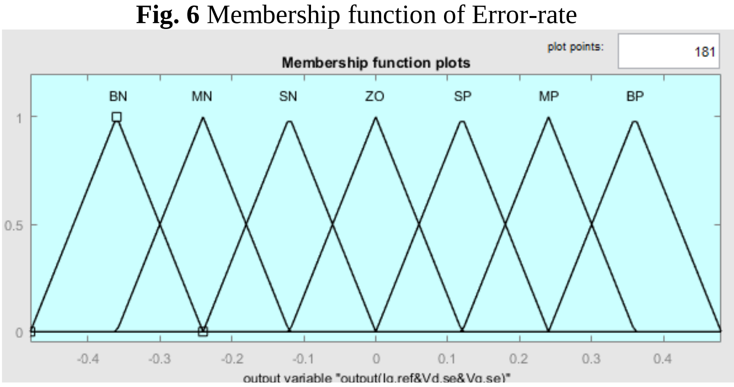


Fig. 7 Membership function of output (*Iq.ref* &*Vd.se* &*Vq.se)*

5. HARMONY SEARCH OPTIMIZATION CONTROL TECHNIQUE

Optimization can be defined as the process of finding best solution or result under given state of affairs. Generally, optimization is used for maximizing or minimizing the value of a function, it may be local optimum or global optimum. In optimization there are different types of problems are being utilized like, Linear optimization, Nonlinear optimization, Dynamic optimization etc. and all have different techniques for solving. In this paper, we have an optimization technique which called Harmony Search (HS) Optimization Control Technique. Harmony Search is a technique which using musical process of searching for a perfect state of harmony. This harmony in music is analogous to find the optimality in an optimization process. In music improvisation process musician plays different notes of different musical instrument and find the best combination of frequency for best tune. Similarly, in HS method also best combination of available solutions is selected and objective function is optimized [8-9]. The HS method had been successfully applied to diverse range of problems. HS algorithm has many advantages over other meta-heuristic algorithms: (a) HS algorithm imposes fewer mathematical requirements and does not require initial value settings of the decision variables. (b) As the HS algorithm uses stochastic random searches, derivative information is also unnecessary. (c) The HS algorithm generates a new vector, after considering all of the existing vectors. Whereas the genetic algorithm (GA) only considers the two parent vectors. These features increase the flexibility of the HS algorithm and produce better solutions. Harmony Search was inspired by the improvisation of Jazz musicians. Specifically, the process by which the musicians (who have never played together before) rapidly refine their individual improvisation through variation resulting in an aesthetic harmony. Steps of harmony search algorithm are shown as flowchart in Figure. In the following five steps:

Step 1. Initialize the problem and algorithm parameters.

Step 2. Initialize the Harmony Memory (HM).

Step 3. Improvise a New Harmony memory.

Step 4. Update the Harmony memory.

Step 5. Check the stopping criterion.

5.1. Initialize the problem and algorithm parameters: In step 1, the optimization problem is specified as follows:
min {f (x) | x ∈ X} subject to g(x) ≥ 0 and h (x) = 0
where, f(x) is the objective function, g(x) the inequality constraint function, and h(x) the equality constraint function. x is the set of each decision variable xi, and X is the set of the possible range of values for each decision variable; that is Xi, min ≤ Xi ≤ Xi, max where, Xi, min and Xi, max are the lower and upper bounds of each decision variable. The HS algorithm parameters are also specified in this step. These are the harmony memory size (HMS), or the number of solution vectors in the harmony memory, harmony memory considering rate (HMCR), pitch adjusting rate (PAR), the number of decision variables (N), and the number of improvisations (NI), or stopping criterion. The harmony memory (HM) is a memory location where all the solution vectors (sets of decision variables) are stored. Here, HMCR and PAR are parameters that are used to improve the solution vector and are defined in step 3.

5.2. Initialize the harmony memory: In step 2, the HM matrix is filled with as many randomly generated solution vectors as the HMS in the following:

$$\mathbf{HM} = \begin{bmatrix} \mathbf{x^1}_1 & \mathbf{x^1}_2 & \dots & \mathbf{x^1}_{N-1} & \mathbf{x^1}_N \\ \mathbf{x^2}_1 & \mathbf{x^2}_2 & \dots & \mathbf{x^2}_{N-1} & \mathbf{x^2}_N \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \mathbf{x_1}^{\mathbf{HMS-1}} & \mathbf{x_2}^{\mathbf{HMS-1}} & \dots \mathbf{x_{N-1}}^{\mathbf{HMS-1}} & & \mathbf{x_N}^{\mathbf{HMS-1}} \\ \mathbf{x_1}^{\mathbf{HMS}} & \mathbf{x_2}^{\mathbf{HMS}} & \dots & \mathbf{x_{N-1}}^{\mathbf{HMS}} & \mathbf{x_N}^{\mathbf{HMS}} \end{bmatrix}$$

5.3. Improvise a new harmony: A new harmony vector, $\boldsymbol{x'} = (\boldsymbol{x'_1}, \boldsymbol{x'_2}, ..., \boldsymbol{x'_N})$, is generated based on three rules:
(1) memory consideration.
(2) pitch adjustment.
(3) random selection.
Generating a new harmony is called 'improvisation'. In the memory consideration, the value of the first decision variable x'_1 .for the new vector is chosen from any value in the specified HM range($\mathbf{x_1}^{\mathbf{1}} - \mathbf{x_1}^{\mathbf{HMS}}$). Values of the other decision variables $(\boldsymbol{x'_2}, \boldsymbol{x'_3}, ..., \boldsymbol{x'_N})$, are chosen in the same manner. The HMCR, which varies between zero and one, is the rate of choosing one value from the historical values stored in the HM, while (1-HMCR) is the rate of randomly selecting one value from the possible range of values.

$$\mathbf{x}_i' \leftarrow \begin{cases} \mathbf{x}_i' \epsilon \{\mathbf{x}_i^{\mathbf{1}} \mathbf{x}_i^{\mathbf{2}} \ \dots \ \mathbf{x_i}^{\mathbf{HMS}}\} \ \boldsymbol{with\ probability\ HMCR} \\ \mathbf{x}_i' \epsilon \boldsymbol{X_I} \ \ \boldsymbol{with\ probability}\ (\mathbf{1} - \boldsymbol{HMCR}) \end{cases}$$

For example, an HMCR of 0.85 indicates that the HS algorithm will choose the decision variable value from historically stored values in the HM with 85% probability or from the entire possible range with (100–85) % probability. Every component obtained by the memory consideration is examined to determine whether it should be pitch-adjusted. This operation uses the PAR parameter, which is the rate of pitch adjustment as follows:

$$\mathbf{x}_i' \leftarrow \begin{cases} \boldsymbol{Adjusting\ Pitch} & \boldsymbol{with\ probabilityPAR} \\ \textbf{Doing Nothing} & \boldsymbol{with\ probability}\ (\mathbf{1} - \boldsymbol{PAR}) \end{cases}$$

The value of (1-PAR) sets the rate of doing nothing. If the pitch adjustment decision for is YES, is replaced as follow:
[Xi'← Xi' ±rand x bw] Where, (bw) is an arbitrary distance bandwidth and (rand) is a random number between 0 and 1.

5.4. Update harmony memory: For each new value of harmony, the value of objective function, f*(x')* is calculated. If the new harmony vector is better than the worst harmony in the HM, the new harmony is included in the HM and the existing worst harmony is excluded from the HM.

5.5. Check stopping criterion: If the stopping criterion (maximum number of improvisations) is satisfied, computation is terminated. Otherwise, steps 3 and 4 are repeated. Finally, the best harmony memory vector is selected and is considered as best solution to the problem.
In the proposed UPFC, there are four controller required. The proposed configuration is done in Matlab Simulink. The Harmony search algorithm is devoted for searching gains of PI controller and FLC parameters in order to minimize the following objective function:

$$\mathbf{Z}= \int_{\boldsymbol{T=0}}^{\boldsymbol{T=T_f}} \boldsymbol{T}\left[\left|\boldsymbol{V_{A_{ref}}} - \boldsymbol{V_{A_{measure}}}\right| + \left|\boldsymbol{I_{q.sh_{ref}}} - \boldsymbol{I_{q.sh}}\right| + \left|\boldsymbol{I_{d.se_{ref}}} - \boldsymbol{I_{d.se}}\right| + \left|\boldsymbol{I_{q.se_{ref}}} - \boldsymbol{I_{q.se}}\right|\right] \qquad \textbf{(5)}$$

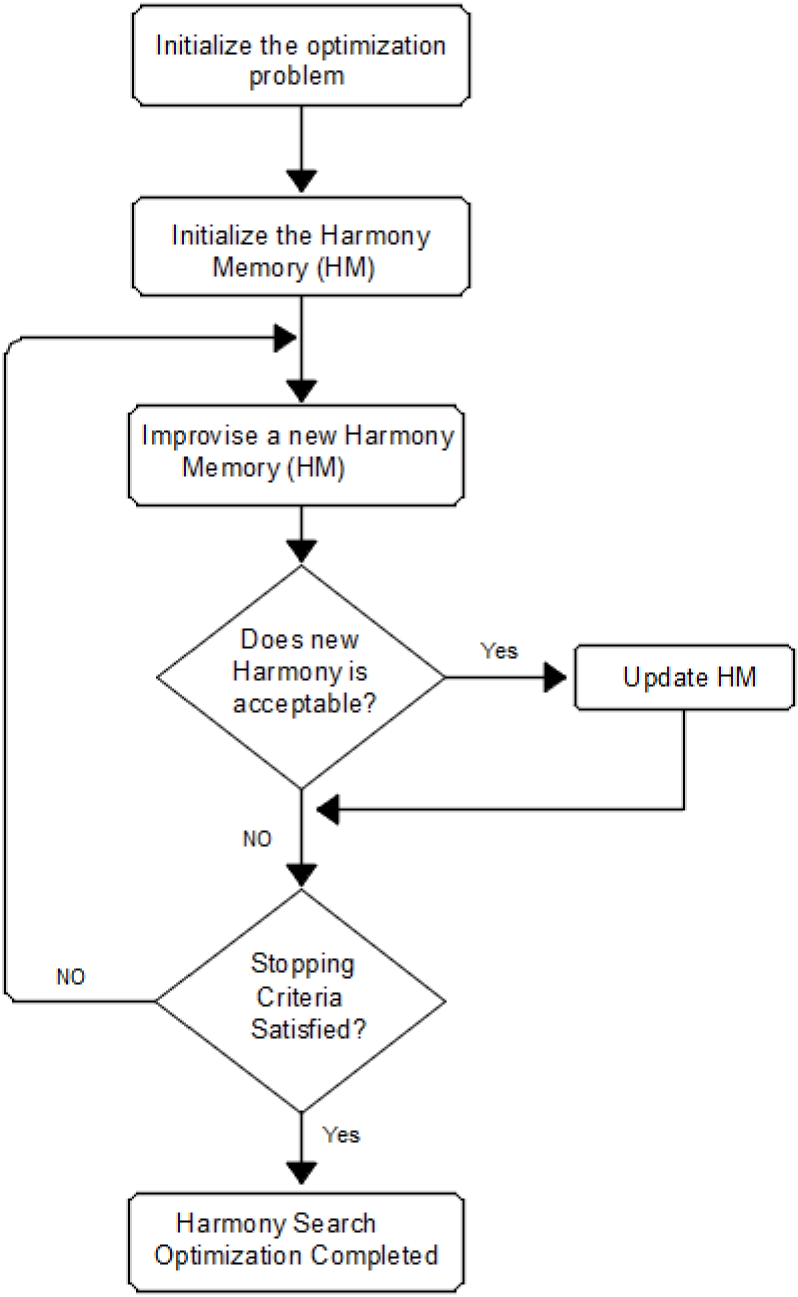


Fig. 8 Flow Chart of Harmony Search Algorithm steps

6. RESULTS AND DISCUSSIONS

In this section, the simulation results for analyzing the performance of the proposed controller is presented. The simulations are conducted for the following three conditions:

1. Under Over Loading operating condition.
2. Under variable loading condition.
3. During Three Phase Short Circuit.

6.1. Under Over Loading operating condition

One of the UPFC advantages is to maintain the line voltage of the transmission network. To study this condition, the response of the proposed controller based UPFC for line voltage at Bus No. 5 is shown in Fig. 10. Here also, the simulation is conducted three times at three cases. Case (a) without UPFC and Case (b) with UPFC based PI controller and case (c) With UPFC based Fuzzy logic controller as shown in Fig. 10.

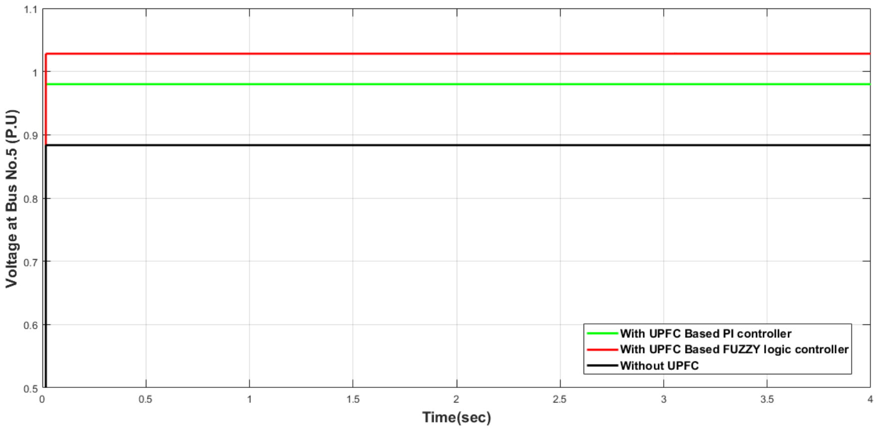


Fig. 10 Voltage at Bus No. 5

The measured value of the line voltage at Bus No. 5 without UPFC were 0.89 p.u. According to Fig. 10, case" b", after Connecting UPFC, the line voltage has reached 0.99 p.u for UPFC based PI controller and this value has become 1.02 p.u for UPFC based FLC. The overall network voltage profile is demonstrated in Fig 11 and it has been observed that with UPFC based FLC the voltages across all the buses of the network have been improved better than UPFC based PI controller.

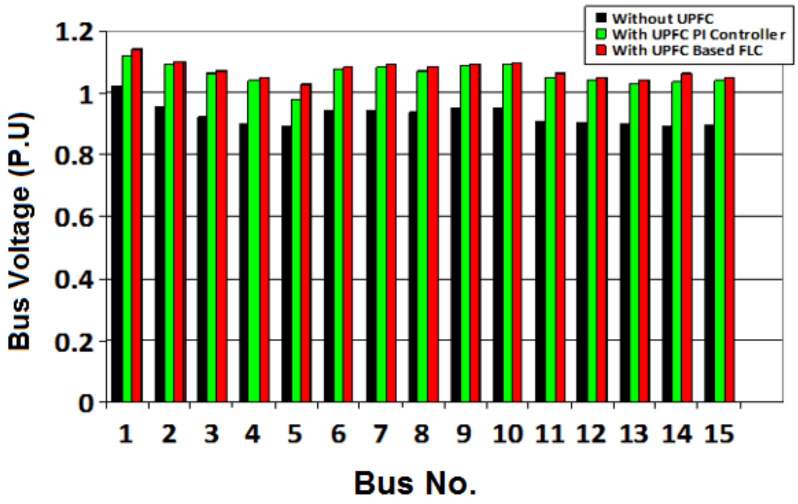


Fig. 11 Voltage Profile across all buses of IEEE 15 Bus Radial system

The response of the Current at Bus No. 5 is shown in Fig. 12. When UPFC was connected to the line 4-5 and the voltage is maintained. The current at Bus No. 5 took 2.42 sec to reach its steady state value when UPFC based PI controller was in operation. However, the current at Bus No. 5 took 1.75 sec to reach its steady state value when UPFC based FLC was in operation.

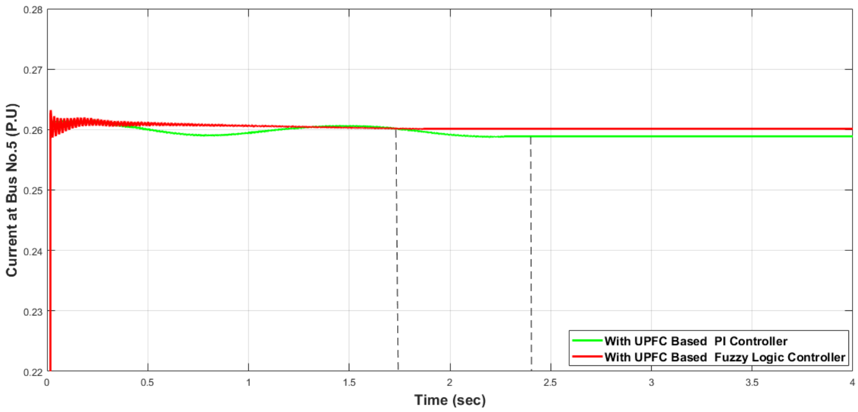


Fig. 12 Load current at Bus No. 5

The response of the DC link capacitor voltage is shown in Fig. 13. When UPFC was connected to the line 4-5. The DC link capacitor was charged up to 9.865Kv at UPFC based PI controller which took 0.7 sec to reach to its steady state value but through Variety changes in its value. However, the capacitor charged to 9.915 kV with a time period of 0.7 sec but smoothly when UPFC based FLC was in operation. For both cases the reference charged value was set to 10 kV.

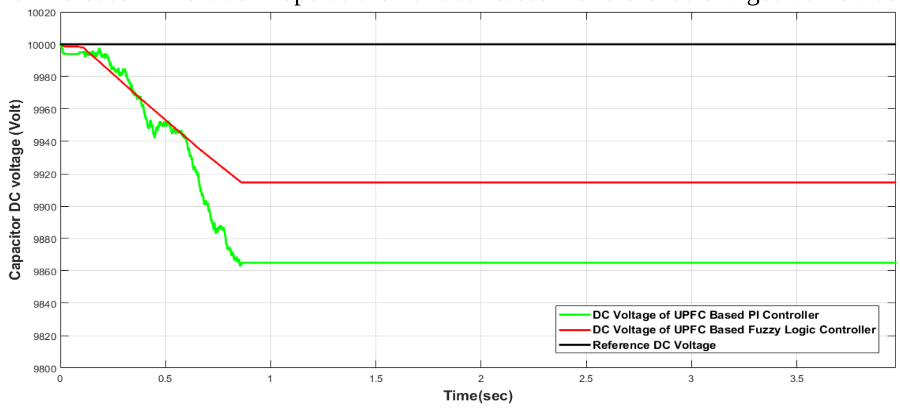


Fig. 13 DC voltage across DC link capacitor of UPFC

The response of Active and Reactive power is shown in Fig. 14 & 15. The reference values of power system parameters for Bus 5 are: active power 0.1647 p.u (494.1 kWatt), reactive power 0.165 p.u (496.98KVAR) and line voltage 1 p.u (11 K Volt). The measured values of active and reactive power flow through the line 4-5 without UPFC were 0.168 p.u (504 k Watt) and 0.171 p.u (513 K Var) respectively. UPFC based on PI controller and FLC are connected to the line 4-5 as shown in Figs. 14 and 15. From Fig. 14, it has been found that with UPFC based PI controller the active power flow was 0.16 p.u (480 k Watt) which has been improved by 4.8% of the nominal value, whereas with UPFC based FLC active power flow has been improved by 9.1% of the nominal value i.e. 0.153 p.u (459 k Watt).

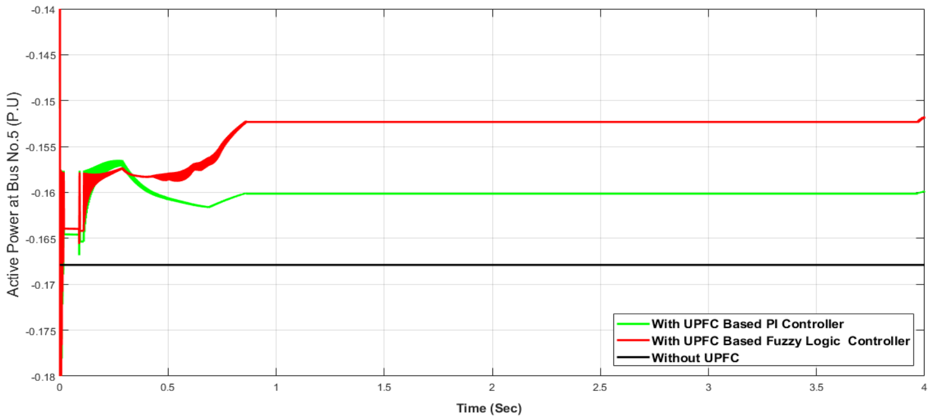


Fig. 14 Active Power at Bus No. 5

From Fig. 15, With UPFC based FLC reactive power flow has reached to 0.155 p.u (465 KVAR) which has been improved by 9.7%. In contrast, reactive power flow over the line with UPFC based PI controller reactive power flow has reached to 0.163 p.u (489 KVAR) which has been improved by 4.85%. And Thus UPFC based FLC has a good performance in control of power flow better than UPFC based PI controller.

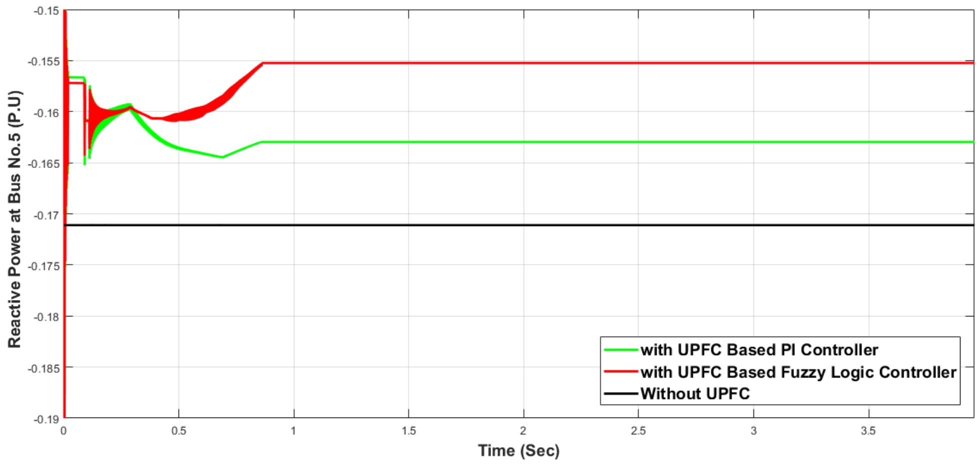


Fig. 15 Reactive Power at Bus No. 5

6.2. Under variable loading condition

The response of the proposed controller based UPFC under load variation has been tested to validate its robustness over a wide range of operating points. Thereby, four loading conditions are considered for simulation. The simulation has run for 4 sec. and each second the load across bus 5 has kept different.

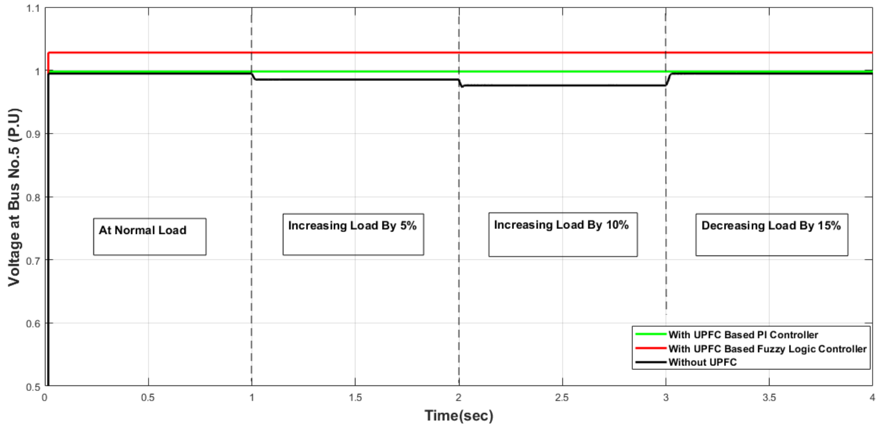


Fig. 16 Voltage at Bus No. 5

It can be observed from Fig.16 that the voltage profile is maintained under various load variation at Bus No. 5. Also Fig. 17 shows the drawing current in different load variations at the same bus. It is clear that UPFC based FLC can maintain the voltage profile better than UPFC based PI controller Thus, proposed FLC based UPFC can work well in different operating points and different load variations.

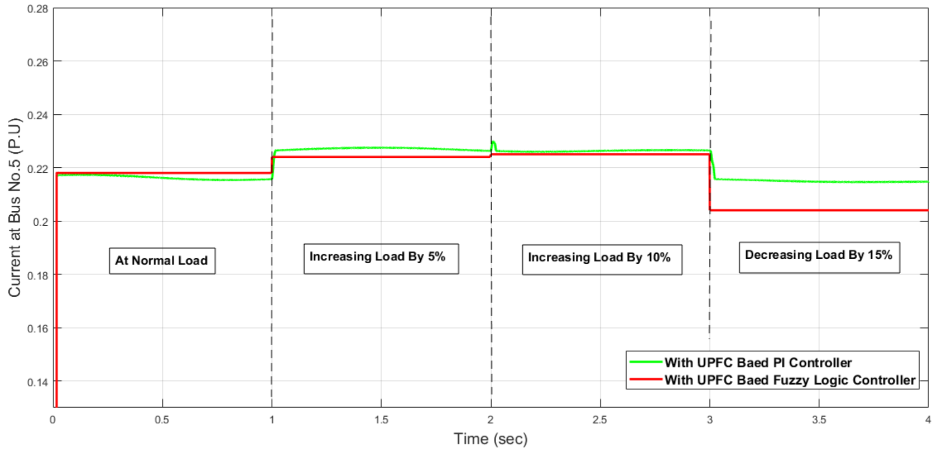


Fig. 17 Load current at Bus No. 5

The measured average values of active and reactive flow through the line 4-5 power under different loading variation without UPFC were 0.154 p.u (462 k Watt) and 0.157 p.u (471 K Var) respectively. UPFC based on PI controller and FLC are connected to the line 4-5 as shown in Figs. 14 and 15. From Fig. 14, it has been found that with UPFC based PI controller the active power flow was 0.16 p.u (480k Watt).whereas with UPFC based FLC active power flow was 0.1525 p.u (457.5k Watt).

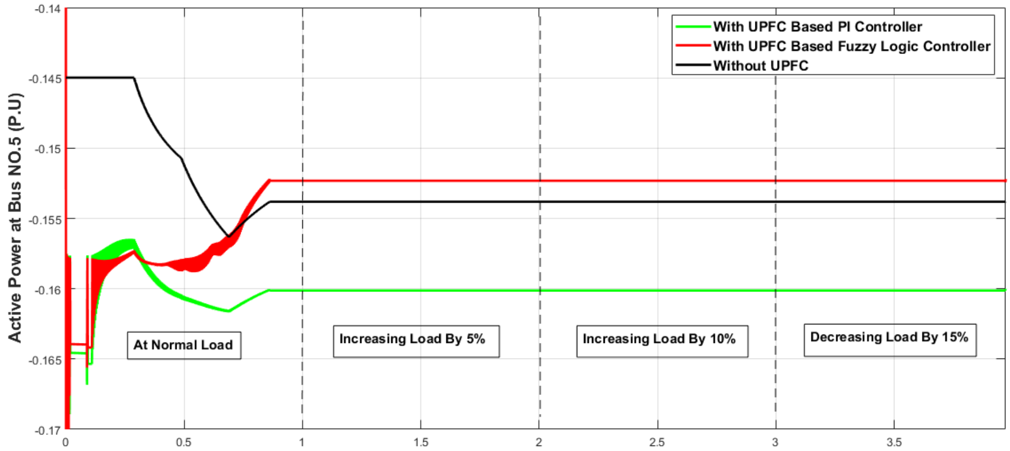


Fig. 18 Active Power at Bus No. 5

From Fig. 19, With UPFC based FLC reactive power flow has reached to 0.155 p.u (465KVAR). In contrast, reactive power flow over the line with UPFC based PI controller has reached 0.1635 p.u (490.5KVAR). And Thus UPFC based FLC has a good performance in control of power flow better than UPFC based PI controller.

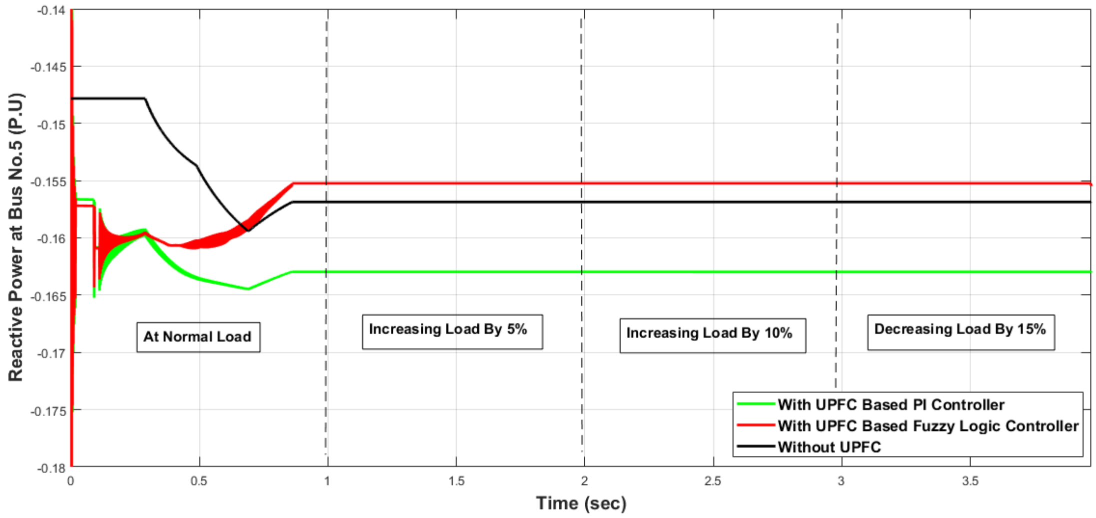


Fig. 19 Reactive Power at Bus No. 5

6.3. During Three Phase Short Circuit

The response of the proposed controller based UPFC during Three Phase Short Circuit at bus No. 5 for (120 m sec) has been tested to validate its robustness at this condition. It can be observed from Fig. 20 that the voltage profile is maintained after Three Phase Short Circuit at Bus No. 5 where UPFC based FLC can maintain the voltage profile to 1.02 p.u whereas UPFC based PI controller maintain the voltage profile to 0.99 p.u. Thus, proposed UPFC based FLC can work well at three phase short circuit condition.

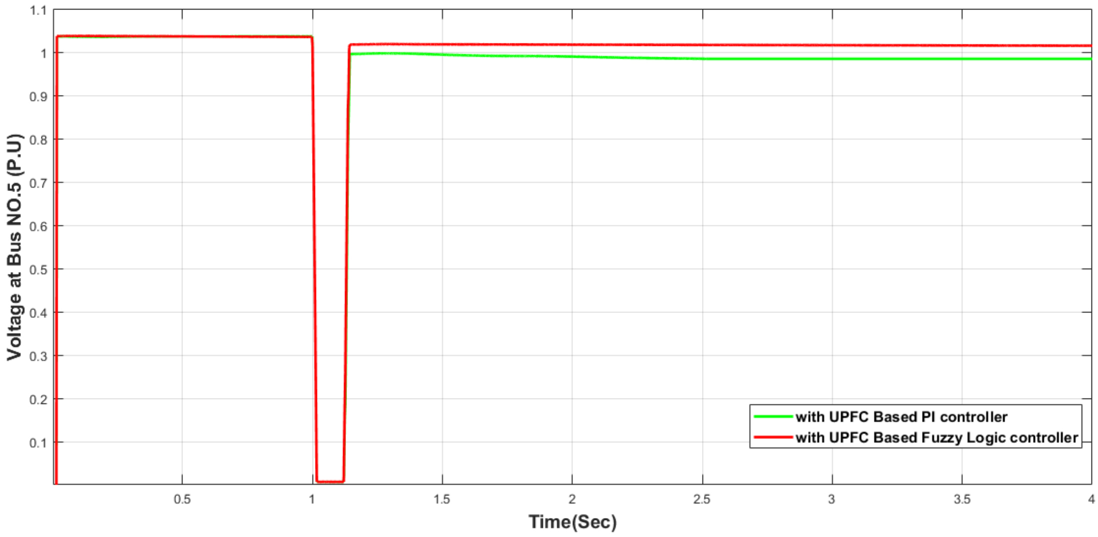


Fig. 20 Voltage at Bus No. 5

The response of the Current at Bus No.1 (generation bus) is shown in Fig. 21. When UPFC was connected to the line 4-5 and the voltage is maintained after occurring three phase short circuit current. The current at Bus No. 1 took 2.85 sec to reach its steady state value when UPFC based PI controller was in operation. However, the current at Bus No. 1 took 1.5 sec to reach its steady state value when UPFC based FLC was in operation. Thus, proposed UPFC based FLC can work well at three phase short circuit condition.

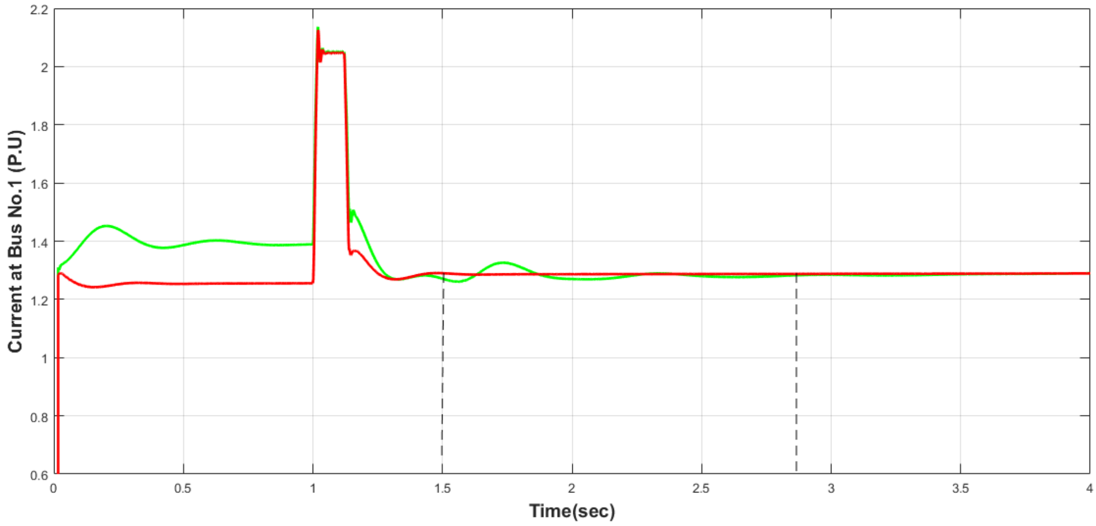


Fig. 21 Load current at Bus No. 1

7. CONCLUSION

This paper has presented real time implementation of a FLC based UPFC to control the transmission line power flow. The proposed controller is validated on IEEE 15 bus Radial system network. The performance of the proposed controller is tested under over loading operation, under load variations, and during three phase short circuit fault. Furthermore, the response of proposed UPFC based FLC is compared to UPFC based PI controller. The results showed that proposed UPFC based FLC has enhanced power flow ability, improved bus voltages and reduced the power losses of the networks more than UPFC based PI controller. Thus, FLC based UPFC has successfully controlled power flow dynamically in transmission line at any mentioned different operating conditions with high accuracy.

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