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CMOS Implementation of Current Mode Analog Multiplier

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ABSTRACT

This paper represents CMOS implementation of improved performance current mode four quadrant analog multiplier. It is based on the translinear loop which builds the squaring operation. The architecture is designed for 90nm CMOS technology with a bias current of 5uA. The architecture consumes a power of 146.9uW with a low supply voltage of 1V having 3dB bandwidth of 450MHz.

Key words: current mode, MOS translinear loop Mode, high bandwidth

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INTRODUCTION

In an Analog Signal Processing Multiplier plays an important role. Thus the designing of Analog Multiplier constitutes a great research area. One of the fundamental building blocks in analog circuit design is the analog multiplier. Multipliers are particularly important in communication and signal processing circuit where they are commonly used for modulation, mixing, phase detection, adaptive filtering, function generators, frequency doubling [1], neural network [2] and fuzzy logic applications. Also Voltage gain amplifier, signal squarer are some application in signal processing. Analog multiplier is used in automatic gain control circuits which are commonly used in RADAR systems and radio receivers. The different architectures were reported by researchers based on different techniques. Also based on the MOS region of operation MOS operating in saturation region, based on sub threshold operated MOS the implementation becomes easier [3-8]. Gilbert based cell, Differential configuration, quadratic equation based and square law characteristics are the different implementation topologies used by the researchers. Most fundamental architectures were originally developed in bipolar technology, where the signal distortion can be kept low across the wide range of frequency [9]. As the digital design has improved, the ability to build analog and digital circuits with a single technology has become increasingly important. To meets mixed signal and low power needs, development of CMOS multiplier architecture has evolved. CMOS technology is better suited for digital circuits than bipolar due to its low processing cost and low power consumption.

Analog voltage multiplication can be performed either by using the linear region characteristics, weak or strong inversion region, square law characteristic of MOS transistors biased in saturation region [10] or by using Gilbert Cell [2, 11-12].

Applying low value of supply voltage is directly translated to lower power consumption in digital circuits. Similar conclusions cannot essentially be drawn for analog circuits design. Power Consumption of the multiplier can be reduce with Low input voltages, low bias currents, low threshold voltages of MOS transistors. Low bias currents and less number of transistors in the design leads to reduced power consumption compared to bias currents in other multiplier architectures [13].

The resistive components of the analog circuits can be controlled by using controlled active devices i.e. second generation current controlled conveyors (CCCCII) and dual X second generation current conveyors (DXCCII).Multipliers based on CCCII & DXCCII have been proposed [14].

Apart from this two modes of operations are used for implementation: voltage mode and current mode. It has been observed that current mode configuration is preferred as it has wide range of input, high linearity, low power consumption.

PRINCIPLE OF OPERATION

Fig1 shows the basic circuit arrangement of MOS forming the squarer circuit realization. The squaring circuit consists of translinear loop which includes transistor M1-M4. The basic translinear principle states that, even number of transistors should be connected in clockwise or in anticlockwise direction, so that the product of current flowing through the clockwise connected transistors will be equal to that of the transistors connected in anticlockwise direction. The drain to source current (I_{DS}) of the MOS transistor operating in saturation region is given as-

$$I_{DS} = K\left(V_{GS} - V_t \right)^2 \quad \text{..... (1)}$$

Squaring on both the sides will give,

$$V_{GS} = V_t + \sqrt{I_{DS}/k} \quad \text{..... (2)}$$

Where V_{GS} is gate to source voltage of MOS, V_t is threshold Voltage, I_{DS} is drain to source current of MOS & K is transconductance parameter equal to

$$K = 0.5\, \mu_0 C_{ox} \left(\frac{w}{L} \right)$$

From the characteristics equation of the translinear principle,

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \quad \text{..... (3)}$$

Substituting equation (2) in (3)

$$V_t + \sqrt{I_{DS1}/k} + V_t + \sqrt{I_{DS2}/k} = V_t + \sqrt{I_{DS3}/k} + V_t + \sqrt{I_{DS4}/k}$$

Since the current flowing through the MOS transistors M1 & M2 is same, therefore $I_{DS1} = I_{DS2} = I_D$

$$2\sqrt{I_D/k} = \sqrt{I_{DS3}/k} + \sqrt{I_{DS4}/k}$$

$$2\sqrt{I_D} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \quad \text{..... (4)}$$

From the fig1,

$$I_D = I_0$$

$$I_{DS3} = I_{out} + I_{in}$$

$$I_{DS4} = I_{out} - I_{in}$$

Thus from the circuit analysis and equation 4

$$2\sqrt{Io} = \sqrt{Iout + Iin} + \sqrt{Iout - Iin} \quad \text{..... (5)}$$

On simplification we get,

$$Iout = Io + \frac{Iin^2}{4Io} \quad \text{..... (6)}$$

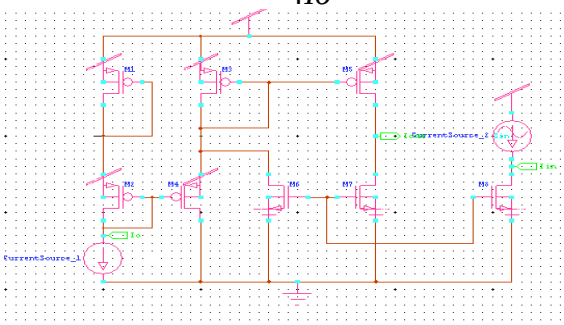

Fig. 1 A Basic Squarer Circuit

The proposed multiplier structure is based on the basic squaring circuit shown in Fig.1. Using the squarer circuit it is possible to implement the multiplier architecture. This implementation consists of two squarer circuits as shown in Fig2. With this arrangement the output current of the multiplier is

$$I_{out} = I_{out2} - I_{out1}$$

Here I_{in1} is $I_1 + I_2$ & I_{in2} is $I_1 - I_2$

Thus on simplification above equation gives

$$I_{out} = \frac{I_1 I_2}{I_0}$$

If I_0 is consider as constant the circuit works as multiplier & if any one of I1 or I2 is considered as constant then works as divider circuit.

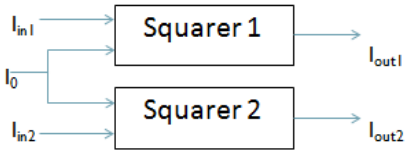

Fig. 2 Proposed Multiplier Circuit Block Diagram

RESULTS

This section describes the function of designed architecture through simulation results.The simulations are done using 90nm CMOS technology. The supply voltage is 1V & dc constant current I0 is 5 µA. Fig 3 & 4 represents the transient and DC simulation results of squarer block.

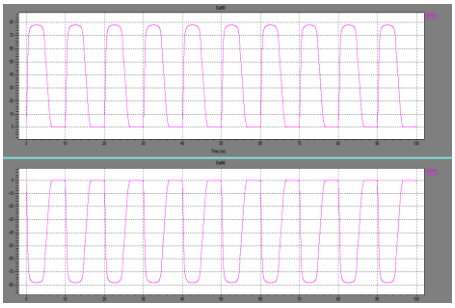

Fig. 3 Transient Result of squarer Circuit

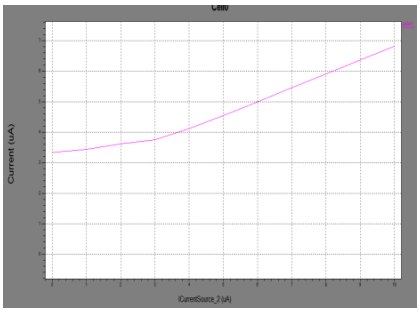

Fig. 4 DC simulation of Squarer Circuit

When the multiplier gets two inputs with same magnitude of two different frequencies, the multiplier results in amplitude modulation. The amplitude modulation is achieved with the modulating signal is 10µA with 100 KHz frequency & the carrier is of 10µA, 2MHz frequency signal. The multiplier transient output waveforms are shown in fig 5.

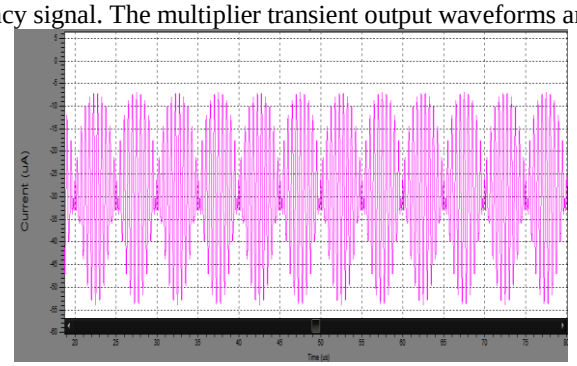

Fig. 5 Amplitude modulator

The multiplier doubles the frequency when it is applied with two inputs of same magnitude & of same frequencies. The fig 6 shows the transient results where both the signals applied are of 10µA in magnitude with 100 kHz frequency.

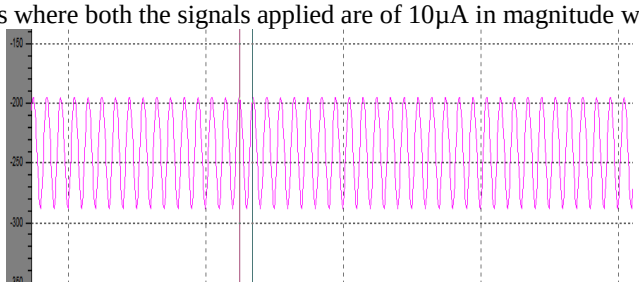

Fig. 6 Frequency Doubler

The AC response of the multiplier is shown in fig 7, where it obtains the 3-dB bandwidth of 450MHz.

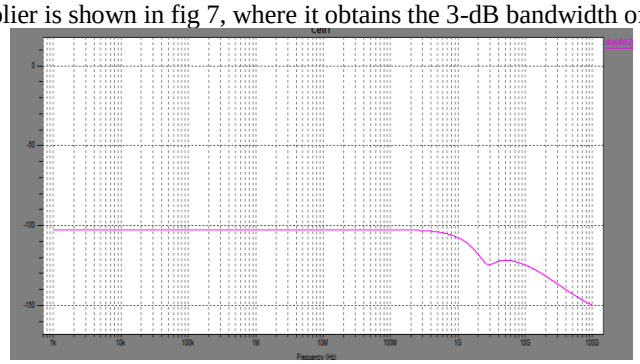

Fig. 7 AC analysis of Multiplier

The designed architecture works efficiently in slow-slow corner as verified from four corner analysis. Fig8 shows the analysis of four corners: FS, FF, SS, SF and TT.

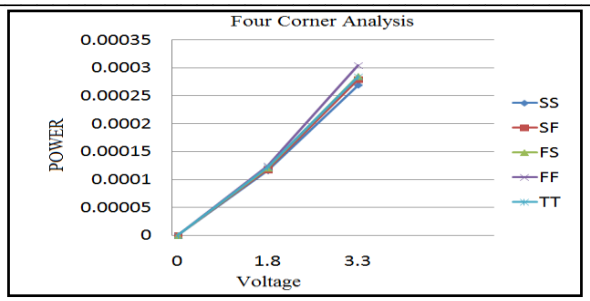

Fig. 8 Four Corner analysis of Multiplier

Fig 9 shows the noise analysis for the designed multiplier architecture. The output voltage in the presence of noise is 6.76491n V/Rt(Hz).

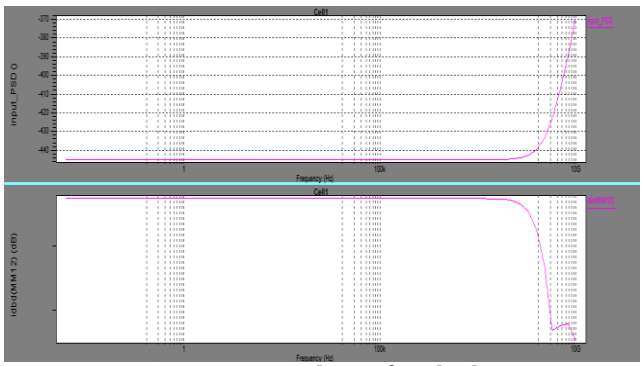

Fig. 9 Noise Analysis of Multiplier

CONCLUSION

The multiplier is designed in current mode configuration at a supply voltage 1V using 90nm CMOS technology. The multiplier achieves a bandwidth of 450MHz with a power consumption of 146.9uW. The designed architecture finds the advantage of its simplicity, accuracy, bandwidth is high and consumes a very low power.

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