



Area Efficient Fixed Width Multiplier Design for DSP Applications

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ABSTRACT

This paper presents an area efficient fixed width multiplier which receives two n -bit numbers and produces an n -bit product. The presented circuit is based on better error compensation bias to reduce the truncation error. Detailed area analysis, delay analysis, Power Delay product analysis between proposed n -bit fixed width multiplier and standard multiplier has been performed. The presented multiplier has been improved & 17.05% area efficient than the standard multiplier. Also the presented circuit finds application in realizing a digital FIR filter provide finest performance.

Key words: Area-efficient, Fixed-width multiplier, High speed, Error compensation bias

INTRODUCTION

In the coming decades, as demands for portable devices, communication system and multimedia are growing, the efficient multiplier plays an important role in VLSI architectures. While implementing multipliers low power consumption, high speed, layout regularity, reduction in area, time and delay are the major concerns which represent the backbone of a DSP system. The practical implementation of algorithms used in many of the communication and digital signal processing (DSP) systems, such as filtering, convolution, fast Fourier transform (FFT), discrete cosine transform (DCT) and hardware implementation of mathematical functions maintain fixed-width operations to avoid the excessive growth in the word length [1-2]. High speed multiplication is one of the requirements of high performance digital system. The fundamental building blocks in most of the multimedia and DSP applications are Parallel multipliers and are repetitive, but they require large computational capability to calculate. Many of the multimedia applications maintain the Fixed-width operations and in most of the cases these results can be interpreted by human assumptions even if they not perfect. This helps to eliminate the need of true product in the multiplier output. The promising solution for this kind of application is fixed width multipliers, which receives an n -bit multiplier operand as well as an n -bit multiplicand operand and computes n -bits output as a product [3-4]. Fixed-width multipliers can be utilized for DSP and multimedia applications to minimize the power consumption by disabling or eliminating parts of the multiplier which results in low switching activity, but introduces certain error in the multiplier output. Post-truncated multiplier is the most accurate approach but require large circuit area. Direct-truncated multiplier is proposed to reduce area overhead, but causes more error in the output. To find the logical balance between area overhead and accuracy these surveys are done.

Constant correction technique and variable correction technique [1, 5-7] are the two different correction techniques proposed to compensate the error introduced in the Fixed-width multipliers with minimal correction logic circuits. Unfortunately, constant correction techniques were inefficient in terms of approximation error. On the other hand, the variable correction techniques proposed as per the survey, significantly improving accuracy. As there are different variable correction methods are available for fixed-width multipliers to optimize error performance, it is quite difficult to conclude that a particular method is suitable for all the applications. In the fixed-width multipliers, researchers introduces a design parameter h , which is varying from $h=0$ to $h=n$, to help the designer to trade-off between the accuracy and area. In this paper we presented better error compensation bias to reduce the truncation error and constructed low error, area efficient fixed width multiplier. The simulated results so obtain as proposed logic gives less area, the comparative delay analysis is summarized in section IV. Section V includes the conclusion.

FIXED WIDTH MULTIPLIER

It is an algorithm for 2's complement array multiplication [1-2]. It is used for signed as well as unsigned numbers. Let us consider two n-bit numbers A and B; they can be represented in 2's complement form as shown below.

$$A = -x_{n-1}2^{n-1} + \sum_{i=0}^{n-2} x_i 2^i \dots\dots\dots (1)$$

$$B = -y_{n-1}2^{n-1} + \sum_{i=0}^{n-2} y_i 2^i \dots\dots\dots (2)$$

The product P= A x B is given by

$$\begin{aligned}
 P &= A \times B \\
 &= \left(-x_{n-1}2^{n-1} + \sum_{i=0}^{n-2} x_i 2^i \right) \times \left(-y_{n-1}2^{n-1} + \sum_{j=0}^{n-2} y_j 2^j \right) \\
 &= x_{n-1}y_{n-1}2^{2n-1} + \sum_{i=0}^{n-2} \sum_{j=0}^{n-2} x_i y_j 2^{i+j} - 2^{n-1} \sum_{i=0}^{n-2} x_i y_{n-1} 2^i - 2^{n-1} \sum_{j=0}^{n-2} x_{n-1} y_j 2^j \dots\dots\dots (3)
 \end{aligned}$$

Equation (3) shows Baugh–Wooley array multiplier [7-10], in which the last two positive terms are subtracted from the first two terms. Instead of subtracting, we can obtain the 2's complement of the last two terms and add them to the first two terms. The last two terms are n-1 bits each that extend in binary weight from position 2^{n-1} up to 2^{2n-3} and the final product is 2n bits and extends in binary weight from 2^0 up to 2^{2n-1} . Each of the last two terms in equation (1) is padded with zeros to obtain a 2n- bit number to be able to add them to the other terms. The padded terms extend binary weight from 2^0 up to 2^{2n-1} . Fig.1 shows the sub product array for 8x8 multiplication. From equation (3), an 8 x8 standard multiplier architecture can be obtained as shown in Fig. 2(b) which are designed using main symbolic cells AFA & NFA and other cells A, ND ,HA and FA denote an AND gate, a NAND gate, Half adder and a full adder, respectively. Device utilization summary is shown in Table 1.

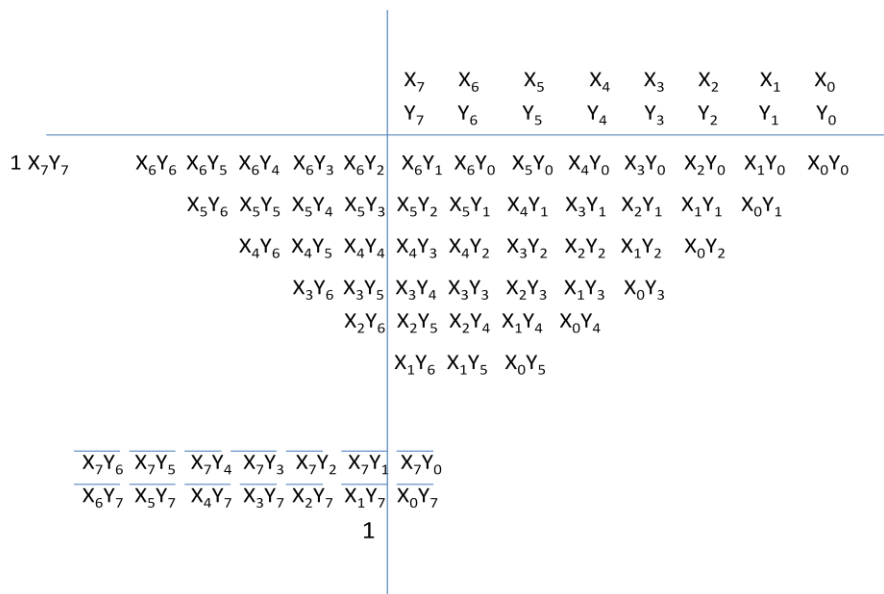


Fig. 1 An 8 x 8 two's-complement multiplier [1]

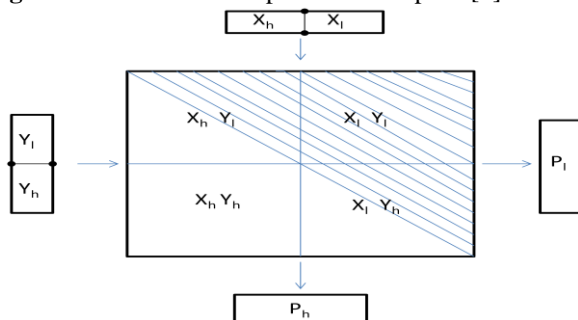


Fig. 2(a) Parts in the parallel multiplier generating the four terms of P. The shaded region represents the truncated cells.

Equation (3) can be written as by partitioning the sub products into two sections,

$$P_{Standard} = MP + LP$$

$$= \sum_{i=n}^{2n-1} P_i 2^i + \sum_{i=0}^{n-1} P_i 2^i \dots\dots\dots(4)$$

where $P_i \in \{0, 1\}$.

$MP = \sum_{i=n}^{2n-1} P_i 2^i$ is the most-significant part, and $LP = \sum_{i=0}^{n-1} P_i 2^i$ is the least-significant part as shown in the upper right triangular area of Fig. 2(a). It is well known that the simplest fixed-width multiplier is to directly truncate LP section, but this approach leads to the largest truncation error. So, Kidambi et al. [2] provided a constant bias method, which was derived from the carry propagation probability of LP.

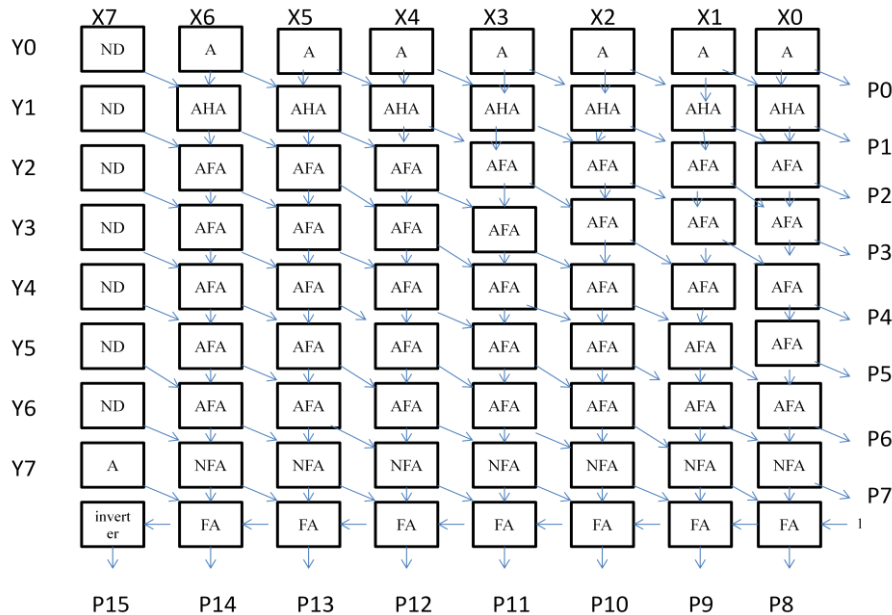


Fig 2. (b) Architecture of the standard multiplier using AFA gate and NFA gate

LOGIC DIAGRAM OF AFA AND NFA

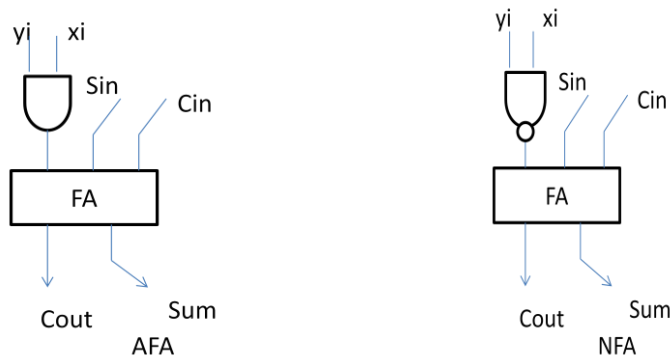


Table -1 Device utilization summary

Logic Utilization	Used
Number of Slice LUTs	33
Number of Occupied Slices	88
Number of bonded IOBs	31
Maximum combinational path delay	12.820ns

The truncated multiplier presented in [1] yields the approximate n-bit fixed-width product P_{K-G-A} ; that is

$$P_{standard} \cong P_{K-G-A} = MP + \sigma_{K-G-A} \times 2^n$$

where σ_{K-G-A} represents the error-compensation bias depending on the width n. While the width n is given, the error-compensation bias σ_{K-G-A} is a constant under the uniform probability distribution of input bits. Although this approach compensates more information than the simplest truncated multiplier, the bias cannot be adaptively adjusted for different input signals. Thus, the truncation error is still large. Jou et al. [7] presented another way to analyze the error compensation, and suggested a truncated multiplier which results in the fixed-width product P_{J-K} as in (6) and (7), where the index $\theta_{J-K} = x_{n-1}y_0 + x_{n-2}y_1 + \dots + x_0y_{n-1}$. Note that the index θ_{J-K} , which is a function of input signals X and Y, determines the error compensation bias σ_{J-K} .

$$P_{standard} = P_{J-K}$$

$$= MP + \sigma_{J-K} \times 2^n$$

$$\sigma_{J-K} = \begin{cases} (x_{n-2}y_1 + x_{n-3}y_2 + \dots + x_2y_{n-3} + x_1y_{n-2}) + 1, & \text{if } \theta_{J-k} = 0 \dots \dots (6) \\ x_{n-2}y_1 + x_{n-3}y_2 + \dots + x_2y_{n-3} + x_1y_{n-2}, & \text{if } \theta_{J-k} > 0 \dots \dots (7) \end{cases}$$

Though the bias σ_{J-K} performs better than the bias σ_{K-G-A} , it is deeply expected to develop a generalized methodology to further improve truncation error [10-13]. It is known that the most accurate truncated product is theoretically given by

$$P_{standard} \cong MP + \sigma_{Temp} \times 2^n$$

$$\sigma_{Temp} \sigma_{Temp} = [LP]_r$$

$$= \left[\frac{1}{2} (x_{n-1}y_0 + x_{n-2}y_1 + \dots + x_1y_{n-2} + x_0y_{n-1}) + \frac{1}{2^2} (x_{n-2}y_0 + \dots + x_0y_{n-2}) + \dots + \frac{1}{2^{n-1}} (x_1y_0 + x_0y_1) + \frac{1}{2^n} x_0y_0 \right] \dots \dots (9)$$

From equation (9) it is cleared that σ_{Temp} is affected due to the largest weights. For evaluating the resulting performance, given inputs X and Y, let ε , $\bar{\varepsilon}$ and v be the absolute error between the standard multiplier and various truncated multiplier, the average error, and the variance of error, respectively [14-15]. That is

$$\varepsilon \square |P_{standard} - P_{Truncated}| \dots \dots (10)$$

$$\bar{\varepsilon} \square E\{\varepsilon\} \dots \dots (11)$$

$$v \square E\left\{\left(\varepsilon - \bar{\varepsilon}\right)^2\right\} \dots \dots (12)$$

Proposed Multiplier Design

The proposed 8×8 lower-error fixed-width multiplier has been designed using basic symbolic cells along with ND-ND cell and A-A cell shown in Fig. (3). Logic diagram of ND-ND cell and A-A cell are given below. Device utilization summary is shown in Table 2.

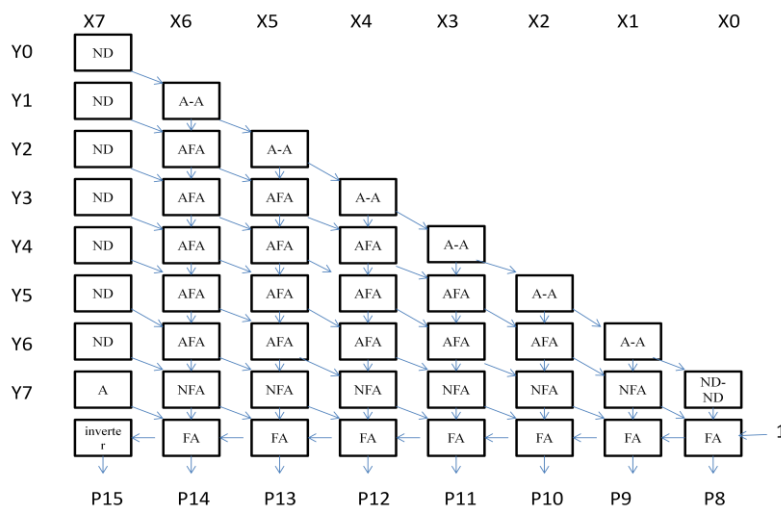


Fig. 3 Proposed lower-error fixed-width 8×8 multiplier

Logic diagram of a-a cell and nd-nd cell

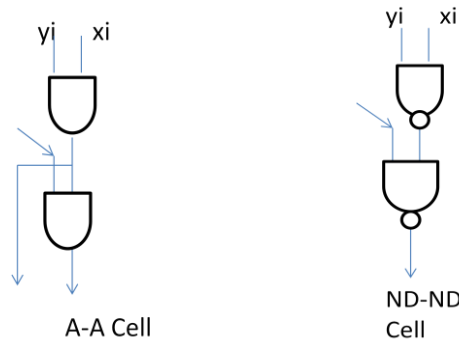


Table -2 Device utilization summary

Logic Utilization	Used
Number of Slice LUTs	29
Number of Occupied Slices	73
Number of bonded IOBs	24
Maximum combinational path delay	11.521ns

PERFORMANCE COMPARISONS AND AREA COMPARISON

In this section, it has been shown that the proposed fixed-width multiplier achieves better performance than the other fixed-width multipliers by computer simulations. The performance is evaluated in terms area, delay and power delay product respectively. Multiplier architecture are simulated using Xilinx Virtex-5 FPGA device XC5VLX110t. Results are summarized in Table 3.

Table -3 Performance Parameter Comparison [Xilinx Virtex-5 FPGA device XC5VLX110t

n - bit	Fixed Width Multipliers	No. of Slices	No. of LUT'S	No. of bonded IOB's	Delay (ns)	PDP(nJ)
		Used/Available	Used/Available	Used/Available		
8	Standard Multiplier	33/3120	88/12,480	31/172	12.820	4.12
	Ref[8] w=2	37/3120	76/12,480	24/172	14.706	4.72
	Proposed Multiplier	29/3120	73/12,480	24/172	11.521	3.7

The comparison results show that our proposed fixed width multiplier is more accurate than the others. The excellent performance is achieved due to the fact that we derive a better error-compensation bias to reduce the effect of truncation error.

CONCLUSION

Fixed-width multipliers can be utilized for DSP and multimedia applications to minimize the power consumption by disabling or eliminating parts of the multiplier which results in low switching activity, but introduces certain error in the multiplier output. This paper presents the method for designing a area efficient fixed width multiplier. Error compensation bias is designed by choosing the generalized index to reduce the truncation error and then construct a lower error, fixed-width multiplier, which is area-efficient for VLSI realization. The result exhibits that the proposed lower error fixed-width multiplier is area efficient than the standard multiplier & Ref [8] w=2 multiplier. Delay in case of Ref [8], w=2 is more than standard multiplier & the proposed one. But it is 17.05% area efficient than the standard one. Similarly 10.13% & 21.66% faster than the standard multiplier & Ref. [8] w=2. In terms of power delay product it improves 10.19% & 21.61% compared to standard multiplier & Ref. [8] w=2.

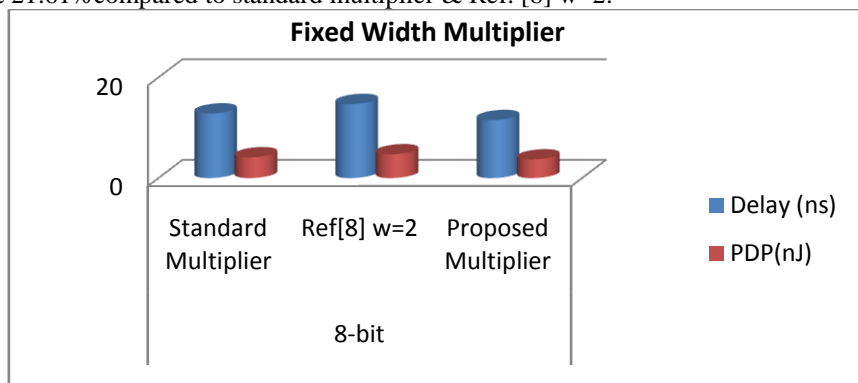


Fig. 4 Comparative Analysis in terms of PDP & Delay

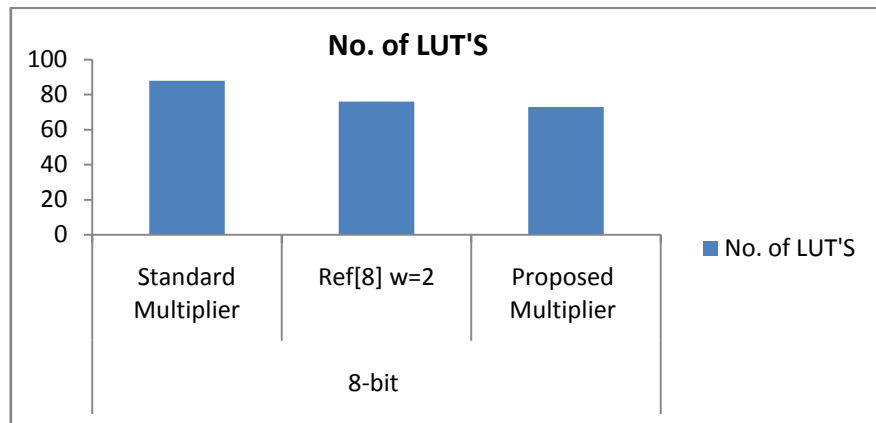


Fig. 5 Comparative Analysis in terms of LUTs

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