European Journal of Advances in Engineering and Technology, 2015, 2(7): 48-55



Research Article

ISSN: 2394 - 658X

Voltage Sag Compensation Capability of IDVR

Gauri S Sarode and Paresh J Shah

Department Electrical Engineering, SSBT's College of Engineering & Technology, Jalgaon, Maharashtra, India sgauri.sarode@gmail.com

ABSTRACT

Power quality requirement is one of the most important issues for power distribution system. Voltage sag and swells are major power quality issue in distribution system due to non linear loads and superconducting devices use in power electronics converters. To compensate these problems, custom power devices are used. Today the custom power device DVR is used to compensate sag and swell but it required real power and reactive power injection in to distribution system. Real power required external energy storage device whereas reactive power generated within the DVR. Capacity of storage unit decides the ability of DVR to compensate voltage sag. To increase the compensation capacity of system, this paper proposed the Interline dynamic voltage restorer concept. IDVR consist of several DVRs, when one of the DVR compensates for voltage sag appearing in that feeder at the same time others DVRs replenish the energy in the common DC link dynamically. The three phases IDVR system for high voltage is design with space vector pulse modulation technique for generation of reference signal. The close loop control scheme is also add the effectiveness in the system while modeling and simulation of interline dynamic voltage restorer. The simulation results obtained for IDVR are analyzed and presented to show the effectiveness and efficiency of the proposed IDVR system.

Key words: DVR, IDVR, SVPWM, Sag, Swell, DC-link

INTRODUCTION

Power quality is of great importance in distribution system, power quality can be essentially influenced by an important factor like quality service. In present era, most of the power quality problems are due to different fault conditions [1, 2]. These several different fault events are spikes or surges, sags, swells, outages, under and overvoltage, harmonics, flicker, frequency deviations, electrical noise, etc. Distribution system is mainly affected by voltage sag and swell. Voltage sags can cause mostly by lightning strokes faults on the transmission or distribution system or by switching of loads with large amounts of starting current such as motors, transformers and huge dc power supply [3]. The voltage swell mainly occurs due to energizing of capacitor banks, shutdown of large loads, unbalanced faults, transients and power frequency surges.

There are different types of custom power devices used in electrical power network to improve power quality disturbances. Each of the devices has its own merits and limitations. For example, the dynamic voltage restorer (DVR) is preferred over the static var compensator (SVC) because the SVC unable to control active power flow [4]. DVR also has a higher energy capacity compared to the SMES and UPS devices. Furthermore, the DVR is smaller in size and cost is less compared to other custom power devices. Based on these reasons DVR is most popular and useful device presently. But the compensation capability of particular DVR, especially for compensating long duration voltage sags, depends on the energy storage device [5]. This storage capability limits the compensation of long duration voltage sag effectively. To solve this, several DVRs are connected to shear a common DC-link is used to protect sensitive loads from voltage sags in distribution system, this concept is named as interline dynamic voltage restorer (IDVR) [6, 7]. This IDVR system would reduces the cost of the custom power device, as sharing a common dc link as reducing the dc link storage capacity significantly compared to that of a system whose loads are protected by bunch of DVRs with separate energy storages [8]. It also compensates the long duration voltage sag effectively. The IDVR system is implemented in the next section as per IEEE 1159 and IEC 60050 standards. In these standards the voltage sag is defined as a decrease in RMS voltage from 0.1 to 0.9 per unit, for duration of 0.5 cycles to 1 minute. Similarly, voltage swell is defined as an increase in RMS voltage from 1.1 to 1.8 per unit of the fundamental frequency with duration from half cycles to one minute.

OPERATING PRINCIPLE OF IDVR

The IDVR system consists of several DVRs in different distribution feeders sharing a common dc-link. A twofeeder IDVR system illustrated in fig. 1 employs two DVRs connected to two different feeders with different voltage level and are originating from two grid substations [3]. When one of the DVRs in this system compensates for voltage sag, the other is operates in power-flow control mode to refill dc link energy storage which is exhausted due to the real power taken by DVR working in the voltage-sag compensation mode [9, 10]. Due to electrical distance between two feeders, it is practical to assume that the voltage sag in Feeder 1 would have a lesser impact on Feeder 2. Therefore these two feeders can be considered as two independent sources and are corresponding to the Thevenin's equivalent impedances ZL1 and ZL2 connected to the buses one and two of their respective feeders as in fig. 1. ZL1 and ZL2 are calculated based on the fault level.



Fig. 1 Schematic diagram of an IDVR in a two feeder system

SIMULATION FOR VOLTAGE SAG COMPENSATION IN AN IDVR SYSTEM

Fig.2 shows the simulation model of proposed system consist of a space vector pulse width modulation (SVPWM) inverter, its control system, injection transformer with the turn ratio 1:1 and the DC link or energy storage device. The principle of operation is described in Fig.1. The programmable three phase source is connected to three phase load through DVR in order to generate sag. When the load on the feeder one is increased load voltage decreases. If decrease in voltage is less than 90% of nominal voltage the voltage sag is detected by reference generator block. Where the three phase a, b, c sag voltage is transform in to the dq0 transformation. A PID (proportional integral derivative) controller determines an error value as the difference between a decrease in voltage and a rated three phase voltage. The controller attempts to minimize the error by adjusting the process through use of a manipulated variable and generate start and stop triggering pulse for PWM inverter. The DC-link is connected to the inverter for injection of appropriate active power with the help of injection transformer. At the same time DVR two in this system operated on the power flow control mode to replenish dc-link voltage [11]. Table I contain the system specifications with their respective values and are used will implement MATLAB/SIMULINK model. As system is design to analyze the performance distribution feeder having rating of 33KV and 66KV feeder. Feeder one is of 33KV rating and feeder 2 in fig. 2 is of 66 KV rating. According to line ratings the impedances are used, the values of these impedances are stated in the table I. To compensate the voltage appearing on these two feeders simultaneously the DC-link storage of high capacity are required. In this system the storage capacity of 35000V is used. As the filter is connected to inverter side the transformer of 1:1 ratio is used.

The pulse for the inverter can be generated using various pulse width modulation techniques. In the proposed system, the pulse for the switch is generated using SVPWM [12]. This is operated on special switching sequence of the upper three power transistors of a three-phase power inverter [13-14]. To implement of this technique is done one the voltage sag is detected, for detecting the voltage sag feed forward dq0 transformation is used [15-16]. This transformation gives the information of the depth, phase shift of the voltage sag with start and end time.

$$\begin{bmatrix} Vd \\ Vq \\ Vo \end{bmatrix} = \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & 1 \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix}$$
(1)

Eq. 1 use to the transform the three phases a, b, c to the dq0. In this transformation, phase a is align with d-axis that is in perpendicular with the q-axis. The ' θ ' is defined by the angle between phase a and d-axis. The control scheme for the proposed system is based on the error signal between the reference voltage and the measured terminal voltage [17-18].



Fig.2. Simulation model of proposed system

Table -1 System Parameters

Specifications	Values	Specifications	Values
supply voltage of feeder1(ph-ph)	33000V	resistance of feeder1	0.1Ω
Supply voltage of feeder 2(ph-ph)	66000V	inductance of feeder1	1.0001e-6
dc-link capacity	35000V	Resistance of feeder 2	500Ω
Injection transformer turn ratio	1:1	Impedance of feeder2	800e-3
Frequency	50 Hz		

RESULTS AND DISCUSSION

The simulations are performed on the IDVR system using MATLAB/SIMULINK. System performance is analyzed for compensating voltage sag with different sag and swell values so as to achieve rated voltage at given load. Various cases of different load condition are considered to study the impact of DC storage on sag compensation. These various voltages sag and swell compensation cases are discussed below:

Voltage Sag Compensation using IDVR System for Feeder 1

Case I: A three phase fault is created by introducing load 2. As a result voltage sag of 10% is generated. The transition time for the fault is considered from 0.3 sec to 0.8 sec. The simulation result without DVR compensation technique for feeder 1 is shown in fig.3. The uncompensated voltage, the compensated voltage, injected voltage in the feeder 1 and the three phase load voltage shown in fig. 3. When the load increases in such way that the voltage sag of 10% is appears on the 66 KV feeder. It is compensated by the IDVR successfully this are shown in fig. 4. The dc-link of capacity 35KV is capable of mitigating voltage sag of feeder 2 and feeder 1 at a same time. The simulation results shows in fig.3 and 4 are stated that the IDVR compensate the voltage sag of 10% on feeder1 and 2.



Fig. 4 Voltage sag compensation by IDVR in 66KV

Case II: Three phase fault is created via the three phase RL load .Which results in voltage sag of 20%. The transition time is from 0.3 sec to 0.8 sec as shown in Fig. 5. The simulation results without compensation are shown in the Fig.5. The compensating voltage sags in feeder1 of IDVR with dc-link voltage. The same result is obtained in case of feeder 2

No. III	n n n	10 000 M	
	AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA	MARKARA MARKA	
and the second se	1 N N		
HEARING	n de Persian	uinan ina ina ina ina ina ina ina ina ina	<u>Brinnan</u>
1			
			-

Fig. 5 20% voltage sag compensation in feeder 1 by IDVR system



Fig.6. Voltages swell compensation in feeder 1



Fig.7 Voltage swells compensation in feeder 2

Voltage Swells Compensation using IDVR System for Feeder 1

Case I: For voltage swell creation the three phase load is cut off. So that the load on the system is decreases and load voltage is increases. The transition time for the fault is considered from 0.3 to 0.8. The simulation result are shows the compensation voltage, uncompensated voltage, load 2 injected voltage and the injected voltage by inverter. The result shown in Fig.6 is for voltage swell of 20%.

Voltage swell compensation on feeder 2 which is of 66 KV are successfully achieved by the IDVR are shown in fig.7. The voltage swell created on the both the feeders are fully compensated by the IDVR system effectively are shown in the fig.6 and fig 7.

Case II: The three phase swell is created on the both the feeder of the magnitude 27 % .transition time for the fault is considered from 0.3 sec to 0.8 sec as shown in fig. 8. When voltage swell of 27% is created on the feeders 2 then the voltage swell of that feeder is successfully compensated by IDVR system and shown in fig. 9.



Fig. 8 Voltage swells compensation by IDVR of magnitude 27%



Fig.9 Voltage 27% swells compensation result for 66 KV feeders.

ANALYSIS OF VOLTAGE SAG AND SWELL COMPENSATION TECHNIQUES

The power system shown in fig.1 is simulated in MATLAB/SIMULINK, for the case I with an addition of load and case II with sudden cut off of load. During normal operating condition, there is normal flow of current through load 1. At initial state, the load 2 is disconnected from system during the time interval from 0 to 0.3 sec and no sag is appearing in the system. During this interval, there is voltage drop in the load voltage as shown in fig. 3. The voltage drop occurs in the feeder when load 2 is added to the supply line at 0.3 sec. now the sag problem occurs during interval from 0.3 to 0.8 sec. therefore the duration required for voltage injection is 0.5 sec. this required voltage is supplied to the system by using the DVR through injection transformer. Whatever the sag is detected is compared with the reference voltage and then with the help of PID controller the gate pulse is generated and sent to inverter. Inverter injects the voltage in system through injection transformer. This injected voltage of inverter is shown in above fig. 3 to 9 and are named as injected voltage. In case I, 10% voltage sag is appear on the supply line for duration of 0.5 sec. this 10% decrease in voltage sag is compensated by injecting real power from dc-link and reactive power from inverter. At the same time the feeder 2 DVR is operated on power flow control mode to maintain the dc-link voltage constant at 35 KV. The injected voltage from load 2 to dc-link is shown in fig. 3 to 9, as per dc link requirement are named as voltage across load 2. If the sag appears on the both the feeders then the compensation of this voltage sag is completely dependent on the dc-link storage device. The proposed system able to compensate the simultaneous occurrences of voltage sags on both the feeders but total 30% of voltage sag is mitigated using this system.

The additional load is removed from the system at 0.3 sec this is shown in fig. 6 to 9 and named as uncompensated voltage. Then the voltage is increases suddenly such increase in voltage is compensated by the restoration system. The voltage sag and swell are created on the system for duration of 0.5 sec in all the cases and mitigates successfully using IDVR system. The proposed system effectively mitigates the sag and swell occurs on both feeders. The analysis stated that the proposed system are able to mitigated voltage sag and swell up to 27% effectively. The created voltage sag and swell are maintained in table II with their respective feeder rating. This sag and swell are mitigated by proposed IDVR system.

%Voltage sag	%Voltage swell	System voltage
10	20	33 KV
10	20	66 KV
20	27	33 KV
20	27	66 KV

Table -2 Percentage of Sag and Swell

CONCLUSION

In this paper, the simulation of IDVR is done using MATLAB/SIMULINK software and its analysis has been presented. Simulation results showed clearly the performance of the IDVR in mitigating voltage sag and swell problems. The IDVR handled the situation without any difficulties and injected the appropriate voltage component to maintain load voltage at its nominal values. Based on analysis of simulated system, it is suggested that the voltage sag and swell up to 27 % are effectively compensated by the IDVR. The effectiveness of the IDVR system for 33KV and 66KV lines is tested in SIMULINK model. In the tested system it is observed that, after a particular amount of voltage sag, the voltage level at the load terminal decreased and it is successfully maintained at its pre-sag value by inserting IDVR. It is also concluded that the IDVR effectively works on different feeder of different ratings.

REFERENCES

[1] PJ Shah, Rakesh Saxena and MPS Chawla, Various Techniques for Improving the Power Quality in Power Supplies, IEEE International Conference on Computational Intelligence, Communication Systems and Networks, **2009**, 58, 23-25.

[2] PJ Shah, Rakesh Saxena and MPS Chawla, Digital Control Technologies for Improving the Power Quality of Power Supplies, *Neural Computing and Applications, Springer Journal*, **2013**, 22 (1), 235-248.

[3] Gauri S Sarode, Paresh J Shah and Rakesh Saxena, Overview of Interline Dynamic Voltage Restorer for Power Quality Improvement, *Australian Journal of Information Technology and Communication*, **2015**, 2 (1),16-20.

[4] Darlan A Fernandes, Fabiano F Costa and Montie A Vitorino, A Method for Averting Saturation from Series Transformers of Dynamic Voltage Restorers, *IEEE Transactions on Power Delivery*, **2014**, 29(5), 2239-2247.

[5] Rosli Omar and Nasrudin Abd Rahim, Modeling and Simulation for Voltage Sags/Swells Mitigation using Dynamic Voltage Restorer, *Proceedings of the Australasian Universities Power Engineering Conference*, 2008, 1-5.
[6] SS Choi, BH Li and DM Vilathgamuwa, Design and Analysis of the Inverter-Side Filter used in the Dynamic Voltage Restorer, *IEEE Transactions on Power Delivery*, 2002, 17 (3), 857-864.

[7] Carl Ngai-Man Ho and Henry Shu-Hung Chung, Implementation and Performance Evaluation of a Fast Dynamic Control Scheme for Capacitor-Supported Interline DVR, *IEEE Transactions on Power Electronics*, **2010**, 25 (8), 1975-1988.

[8] A Teke, K Bayindir and M Tumay, Fast Sag/Swell Detection Method for Fuzzy Logic Controlled Dynamic Voltage Restorer, Generation, IET Journal of Transmission & Distribution, **2010**, 4 (1), 1–12.

[9] G Justin Sunil Dhas and T Ruben Deva Prakash, A Novel Approach for Voltage Sag Mitigation using Facts Device Interline Dynamic Voltage Restorer, *IEEE 3rd International Conference on Electronic Computer Technology*, **2011**, 4 (8-10), 37-41.

[10] Suma Jothibasu and Mahesh K Mishra, A Control Scheme for Storage less DVR based on Characterization of Voltage Sags, *IEEE Transactions on Power Delivery*, **2014**, 29 (5), 2261-2269.

[11] Laszlo Gyugy, Kalyan K Sen and Colin D Schauder, The Interline Power Flow Controller Concept: A New Approach to Power Flow Management in Transmission Systems, *IEEE Transactions on Power Delivery*, **1999**, 14 (3), 1115-1123.

[12] Zhan, VK Ramachandaramuthy, A Arulampalam and C Fitzer Barnes, Dynamic Voltage Restorer based on Voltage Space Vector PWM Control, *IEEE Sixteenth Annual Applied Power Electronics Conference and Exposition*, **2001**, 2 (1), 1301-1307.

[13] P Ananthababu, B Trinadha and K Ram Charan, Performance of Dynamic Voltage Restorer against Voltage Sags and Swells using Space Vector PWM Technique, *IEEE International Conference on Advances in Computing, Control, and Telecommunication Technologies*, **2009**, 206-210.

[14] Behrooz Mirafzal, Mahdi Saghaleini and Ali Kashefi Kaviani, An SVPWM-based Switching Pattern for Stand-Alone and Grid-Connected Three-Phase Single-Stage Boost Inverters, *IEEE Transactions on Power Electronics*, **2011**, 26 (4), 1102-1111.

[15] Serkan Dusmez, Ling Qin and Bilal Akin, A New SVPWM Technique for DC Negative Rail Current Sensing at Low Speeds, *IEEE Transactions on Industrial Electronics*, **2015**, 62 (2), 826-831.

[16] Ahmed M Massoud, Shehab Ahmed, Prasad N Enjeti and Barry W Williams, Evaluation of a Multilevel Cascaded-Type Dynamic Voltage Restorer Employing Discontinuous Space Vector Modulation, *IEEE Transactions on Industrial Electronics*, **2010**, 57 (7), 2398-2410.

[17] P Usha Rani, Modeling and Simulation of Interline Dynamic Voltage Restorer using SVPWM Technique, *Journal of Theoretical and Applied Information Technology*, **2014**, 60 (1), 34-38.

[18] R Sudha, P Usharani and S Rama Reddy, Digital Simulation of an Interline Dynamic Voltage Restorer for Voltage Compensation, *IEEE International Conference on Computer, Communication and Electrical Technology*, **2011**, 388-396.