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European Journal of Advances in Engineering and Technology, 2023, 10(9):57-60

Research Article ISSN: 2394-658X

Power Gating Implentation for Low Power Optimizations using Gates

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ABSTRACT

Modern days need modern solutions, with the urge in the demand to lower the dissipated power. The integrated circuits with low power VLSI applications prefer a circuit design offer low power while in sleep without any performance degradation. One way to reduce the dissipated power is by using power gating.

Keywords: power gating, dynamic power, isolation cell, transistor sizing, low leakage

1. INTRODUCTION

The recent advancements in technology have put power optimization is the spot light, making it one of the prerequisites for advanced multi core circuits. The power mainly has two components, static power and dynamic power. The static power is generated because of the leakage and dynamic power is generated due to the frequency and voltage activity, also the major factor for power optimizations. Such designs strive to maintain the throughput of the design and also lower the leakage power by shutting down the inactive portion of the design using the logic of power gating.

$$P_{Total} = P_{Dynamic} + P_{Static}$$

$$P_{Total} = \frac{1}{2} C_L V_{dd}^2 \alpha f + I_{sc} V_{dd} + I_{static} V_{dd}$$

Figure 1: Power Formula

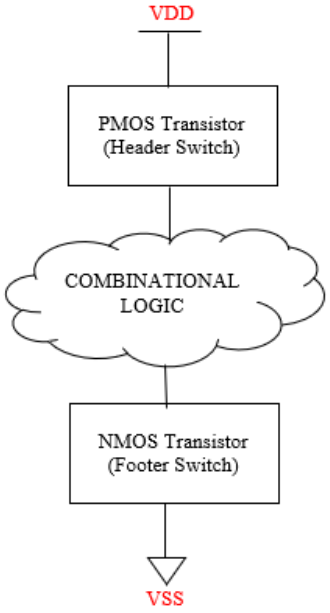

Figure 2: Power Gated Logic Circuit

Power gating is a concept implemented as a part of the circuit sub-system design to reduce the power consumption by cutting off the current to a block of the non-utilized circuit to allow it to rest in sleep, thereby lowering the leakage or stand-by power. Typically, CMOS switches are used to lower the power discharge of the blocked circuitry but consume larger threshold voltage. In addition, low-leaky PMOS transistors have been in

consideration due to lesser area size and same capabilities or NMOS footer switches can also be used similarly to sleep transistors.

Furthermore, power gating can be performed externally and internally. In external mode of operation, the basic power supply to the circuit is switched off, disabling the functionality. Rather, in internally mode of operation, the switches are designed specifically to suit the circuit blocks and shut off the design in small intervals of time.

2. FACTORS OF POWER GATING

Before you begin to size the gate, first we need to determine the worst case scenario for power gate switching. The worst case vectors help in modulating the situation and dynamically size the gate. A few constraints like timing, functional and current constraints also need to be advocated for working of the circuit design without any latencies.

The system needs to be battery operated, the primary reason for low power operations. For potential utilization of power gating, it is best to combine with voltage islands. But it requires a level shifter to balance the signal crossing between the two voltage islands.

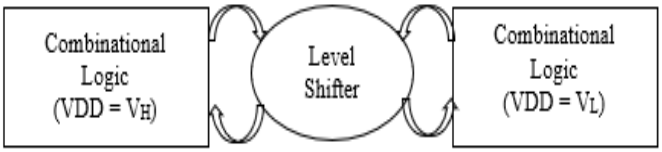

Figure 3: Voltage Island – Level Shifter

As mentioned earlier about the ways to implementing gating is either externally or internally. In order to achieve either of these, the transistors connected to the power need to be sized according to the requirements. Few other parameters are also deployed along with sizing as elaborated:

- Capacitance – The switching capacitance can be regulated to achieve the best circuit integrity by concising the transient current.
- Slew Rate – The most vital parameter in power gating. The slew rate determines the efficiency of gating, as the slew rate increases the efficiency of power gating reduces, making it indirectly proportional to power gating. In accordance with efficiency, a gate control signal can be implemented to monitor the slew rate.
- Gate Size – Based upon the value of the switching current, the capictor value of the switching capacitance is determined. In turn, this switching capacitance leads to designing the size of the gate. Ideally, the size of the gate is cosidered to be around 3.2 times of the switching capacitance. As known fact, the NMOS size is relatively smaller than PMOS, so NMOS footer switcher can provide better area cost and similar performance.
- Leakage Cells – Considering low leakage cells into the design would help reduce the static current, the main parameter leading to higher power values. In general, PMOS header switches have low leakage comparatively benefiting the power reduction.

Considering eachof these individual parameters while desiging the gate would lead to better implementation.

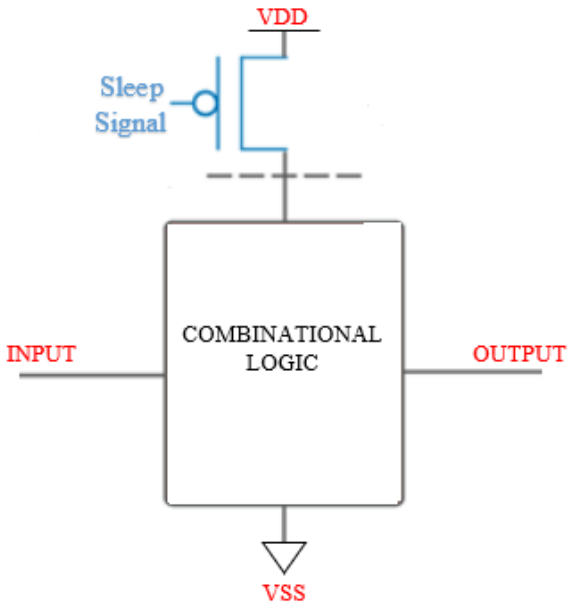

Figure 4: PMOS Header Gate Switch

Further, the delay of these header and footer switch is determined based on the sizing of the gate. During the transition mode the delay of these switches should be minimum and should embrace low leakage while in sleep.
Figure 4 and Figure 5 depict how header and foot switch can be used individually to perform power gating, but a combination of both the switches can also be implemented.

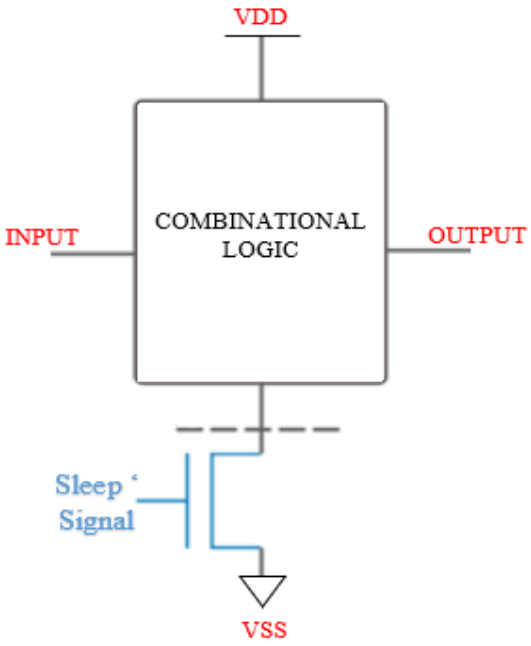

Figure 5: NMOS Footer Gate Switch

3. IMPLEMENTATION

Fine-Grain Power Gating
The fine grain power gating implements a footer switch or header switch as shown in figure 4 and figure 5, integrated as a part of the standard cell design i.e. combinational logic. The transistor is designed using library IP vendor or as a part of the standard cell RTL design code. Further, the VDD power supply or ground supply is also included as a part of the standard cell design.
EDA tools can be directly used to implement the logic of the transistor, making it one of the most convenient methods of implementing. This helps to reduce the leakage power by turning off the idle portions of the circuit. Another important consideration while implementing fine grain power gating, the use of low Vthreshold cells, to reduce the impact of the area of the gating transistor as discussed in the above section of switching capacitance increasing with high switching current.
Coarse-Grain Power Gating
This method of approach implements a grid distribution of sleep switching transistors in the design to balance the power gating logic via shared power network grid. Such an implementation potentially desensitizes PVT variations reducing IR drop fluctuations too. The grid can be implemented in multiple ways.
Ring Based – The sleep cells are placed only on the perimeter of the macro block enabling switching for the blocks closer to the ring.
Column Based – The higher metal layers would be composed of the global power network distribution whereas the lower layers would be composed of the sleep cells network distribution.

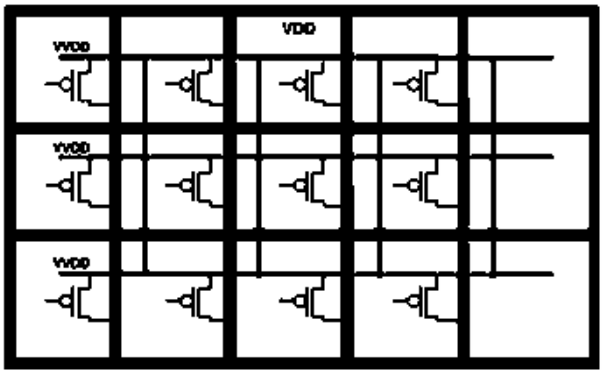

Figure 6: Colum Based Power Gating

Isolation Cells

As the name suggests, the isolation cells are generally implemented to isolate the always on combinational logic versus the power gate switching cells. These cells are the buffer cells with a control signal, enabling the signal would activate it to act like a buffer cell. In contrary, when the control signal is disabled, the cell provides either 1 or 0 as the output.

The isolation cells store the value while acting as buffer cells when the sleep signal is enabled and the combinational circuit is power gated, rather than discarding the output in this state. To comply with the situation, the control signal to the isolation cells is also monitored by the power gate.

4. CHALLENGES

Power gating might stand out to be one of the potential techniques to optimize power consumption and lower the leakage power but has its own complexities.

a. In low leaky situations, the transition power between the on and off state consumes more than the leakage power.
b. Additional cells are required to store the transitioning output before the final output is produced due to power gating, this leads to area and routing penalty.
c. Timing of the power gating switches need to have additional wakeup signal to enter and exit the sleep cycle without any skew.

5. FUTURE SCOPE

Intensive optimization of the transistors performing switching can be implemented using the fake via method. This method specifically adds an additional resistance to the transistors to improve the VDD and ground connectivity.

Further DFT based power gates can also be installed during the testing mode, to improve the controllability of the design.

6. CONCLUSION

The impact of reducing leakage power has been of tremendous advantage to the semiconductor industry. The rise in the trend to reduce the technology scaling to gain area and power efficiency would benefit highly with the implementation of power gating with minimum area trade off.

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