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A Systematic Literature Review of Advanced Packaging Technology in Semiconductors: Revolutionizing the Industry

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ABSTRACT

Semiconductor packaging is vital in ensuring the environmental protection and reliable interconnection of semiconductor chips, serving as the crucial first level of packaging in the electronic device manufacturing process. This systematic literature review delves into the evolution and impact of advanced packaging technologies (tech.s) within the semiconductor industry. The research investigates how these advancements have contributed to enhancing semiconductor devices, influencing industry trends, and shaping the future Landscape. The study comprehensively analyzes a wealth of literatures, providing insights into the multifaceted aspects of advanced packaging. It explores the intricate balance required to meet diverse performance requirements, including considerations for physical, mechanical, electrical, and thermal aspects. The semiconductor package's role in addressing mechanical stresses, environmental factors, and electrostatic discharge during handling and mounting is examined. Furthermore, the paper investigates its pivotal role as a mechanical interface for testing processes and facilitating the next interconnection level.

Through a thorough examination of industry trends, the research illuminates the trajectory of advanced packaging tech.s. Graphs and charts are utilized to illustrate key findings, offering a visual representation of the dynamic evolution within the semiconductor packaging domain. The paper also scrutinizes the specifications for quality, reliability, and cost-effectiveness, essential factors in the successful deployment of semiconductor packages.

As semiconductor devices continue to evolve, the insights derived from this systematic literature review provide a valuable understanding of the current state and future prospects of advanced packaging tech.s. The findings contribute to the ongoing discourse on semiconductor industry advancements, offering a foundation for informed decision-making and further research initiatives in this dynamic field.

Key words: Advanced packaging technology, semiconductor industry, 2.5D packaging, along with 3D packaging, along with fan-out wafer-level packaging, system-in-package, performance metrics, miniaturization, power efficiency, industry trends.

INTRODUCTION

Semiconductor packaging technologies: An Overview

The evolution of semiconductor packaging tech.s has been a critical driver for the electronics industry, shaping the landscape of electronic devices over the decades. In the early days, Dual Inline Packages (DIPs) dominated, utilizing through-hole tech. for pin insertion into Printed Wiring Boards (PWBs). However, as the demand for higher density, smaller form factors, and enhanced performance emerged, packaging tech.s underwent significant transformations **(Ahn, & Bhattacharya, 2018).**

- Transition to Quad Flat Packages (QFP) and FC-BGA (Flip Chip-Ball Grid Array)
  By the mid-1970s, QFPs took center stage, introducing solder reflow tech.s on PWB lands to achieve narrower pin pitches. Simultaneously, the emergence of FC-BGA addressed the escalating pin counts in logic semiconductor packages, particularly in Micro Processing Units (MPUs). FC-BGA, with solder

balls formulated at the package's back for area array packaging, became a driving force for pitch reduction and package miniaturization.

- Copper-Clad Laminates and Organic PKG (Packaging) Substrates
  Logic semiconductor packages predominantly relied on ceramic substrates until around 1993 when advancements in highly temp.-resistant copper-clad laminates along with build-up wiring tech. create organic PKG substrates viable. Organic substrates met the industry's demands for faster clock frequencies, fine-pitch wiring formation, and cost-effectiveness. Organic materials' low permittivity facilitated high-speed signal transmission, making them suitable for mounting Micro Processing Units (MPUs) in computers **(Ahn, & Bhattacharya, 2018).**
- SiP Technique and 3D Packing Advancements
  In response to the growing demand for faster, thinner, and smaller electronic devices, the SiP tech. emerged. SiP integrates multiple semiconductor devices right into a single package, achieving notable advancements, especially in 3D packing tech.s. This innovation involves stacking different semiconductor packages and chips, reflecting the industry's pursuit of compact, power-efficient products, exemplified by the proliferation of smartphones and mobile electronic terminals **(Lai, & Wong, 2020).**
- Post-Moore's Law Era and Emerging Packaging Technologies
  The semiconductor industry, having grown into a multi-trillion-dollar market, now faces challenges in manufacturing tech.s reaching physical size limits. In the post-Moore's Law era, researchers explore alternative materials and structures, such as carbon nanotubes/graphene and heterogeneous integration (integ.), to sustain or surpass the pace set by Moore's Law. Emerging tech.s like power electronics and (Light Detection and Ranging) LiDAR for automobiles play significant roles, necessitating packaging tech.s to keep pace with the increasing demand for high-speed and high-bandwidth computation **(Kim, & Kim, 2019).**
- System-in-Package (SiP) Technology in the Post-Moore's Law Era
  The iconic Moore's Law, a cornerstone of the chip industry, appears to have reached a bottleneck due to ongoing advancements in integrated circuit tech. As a response, the industry has turned its attention to (SiP) tech., which integrates active and passive devices into a single package, creating a system-level device. SiP operates at the packaging's integ. level, complementing other integ. levels like chip-level (SoC) and board-level (PCB). **(Kim, & Kim, 2019).**
- SiP, Chiplet, and Advanced Packaging
  SiP tech., building upon the System-on-Chip (SoC) design, operates in 2D, 2.5D, or 3D configurations, reflecting the diverse goals of electronic integ. Alongside SiP, the concept of Chiplets has emerged, representing small chips or cores interconnected through advanced packaging tech.s. Some consider Chiplets an extension and expansion of the SiP, highlighting the intertwined nature of advanced packaging tech.s **(Kim, & Kim, 2019).**

Current Landscape and Challenges

In the present day, semiconductor packaging tech.s play a crucial role, with increasing emphasis due to the demands from the device along with system ends. While the past saw packaging as a less critical aspect, contemporary developments require more focus on addressing issues related to package tech. The industry explores ways to meet performance demands while managing the challenges posed by various packaging and interconnection tech.s **(Zhang, & Wong, 2021).**

Wire Bonding and Flip-Chip Processes

The wire bonding process, a fundamental aspect of semiconductor packaging, has evolved over the past 40 years, with noteworthy improvements in equipment and materials. Automation has replaced manual operations, and materials are engineered for particular characteristics along with applications. Flip-chip tech. represents a departure from wire bonding, starting with a bumped wafer and involving die attach adhesive and wire bond replacement with pick-and-place and reflow. The encapsulation also differs, with underfill commonly replacing molding compound **(Zhang, & Wong, 2021).**

Equipment

Figure 1 depicts a transfer mold press that is employed to enclose plastic packaging using molding compound. Almost all the procedures outlined in Table 1, which illustrate the process of assembling and producing semiconductor packages, already employ automated machinery for large-scale production. Notable examples include the die bonder, along with the wafer saw, along with the wire bonder.

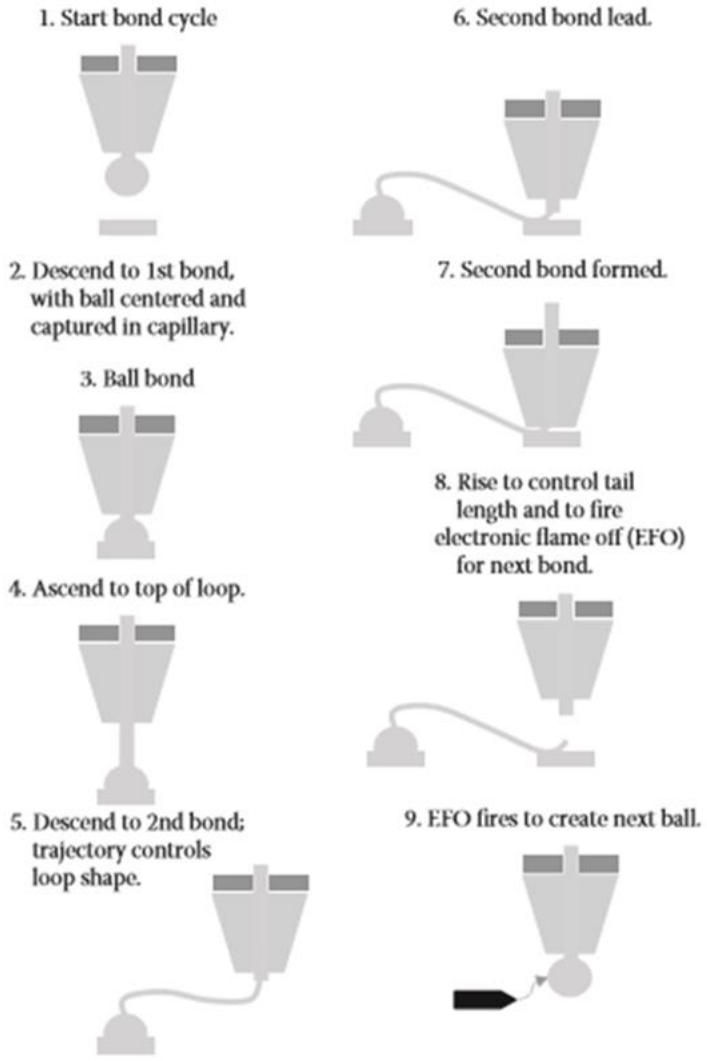

Figure 1: Process steps in gold thermosonic wire bonding (Zhang & Wong 2021)

Table 1: Wire Bond. Versus Flip-Chip Process Flows for a (Di Cino, & Li, 2022).

Wire Bond	Flip Chip
Wafer	Wafer
Dice	Wafer bumping
Die attach	Dice
Cure	Pick and place plus flux
Wire bonding	Reflow
Encapsulate	Underfill encapsulation
Ball attach	Ball attach
Mark	Mark
System test	System test

MATERIAL INTERACTIONS

The semiconductor package consists of various components that exhibit significant variations in physical characteristics, as illustrated in Table 2. The crucial aspect is to identify the most rational material composition that is both cost-efficient and feasible for large-scale production.

Table 2: Key Properties of Semiconductor Packaging Materials (Di Cino, & Li, 2022).

Material	CTE (ppm / °C)	Density (g/cm^3)	Thermal Conductivity ($W/m^* K$)	Electrical Resistivity ($\mu\Omega - cm$)	Tensile Strength (GPa)	Melting Point (°C)
Silicon	2.8	2.4	150	N/A	N/A	1430
Molding Compound	$18 - 65$	1.9	0.67	N/A	N/A	$165(T_g)$
Copper	16.5	8.96	395	1.67	$0.25 - 0.45$	1083
Alloy42	4.3	N/A	15.9	N/A	0.64	1425
Gold	N/A	19.3	293	2.2	N/A	1064
Aluminum Eutectic	23.8	2.80	235	2.7	83	660
Tin-Lead Solder	23.0	8.4	50	N/A	N/A	183
Alumina	6.9	3.6	22	N/A	N/A	2050
Aluminum nitride	4.6	3.3	170	N/A	N/A	2000

THERMAL MANAGEMENT

Efficient thermal management is crucial for semiconductor packages, especially in facilitating the ongoing enhancements of microprocessors (Yang et al., 2020). The primary objective is to create smaller devices capable of operating at greater power along with frequencies, exceeding 65 GHz **(Li et al., 2010).** As the power density along with current levels of said devices increase, issues like on-chip hotspots along with Joule heating become prominent. Failure to minimize operating temperatures can lead to thermal degradation or catastrophic failure, with both failure rates along with gate delay escalating with temperature. Hence, the package's thermal controlling capability is vital for ensuring product dependability along with quality.

Thermal management procedures can be broadly categorized into passive along with active methods **(He, Yan, & Zhang, 2021).** Passive tech.s, which do not require input power, include system-level approaches like natural radiation/convection optimization, along with heat conduction, along with phase change. On the other hand, active tech.s, which demand input power, encompass methods like external forced convection, along with pumped loops, along with refrigeration at the system level. Typically, passive systems are known for their reliability and easy installation but may lack performance. In contrast, active systems offer raised performance but come with lower reliability and added complexity. Also, these conventional tech.s are now becoming outdated and are insufficient for effectively managing thermal challenges in advancing electronics.

To meet the evolving demands of great-performance electronics, there have been significant progressions inside microscale thermal management (MTM) systems. Also, these innovative in-package systems are designed to provide enhanced spot cooling for critical great heat flux regions, like the device junction. This shift towards MTM represents a critical step in addressing the thermal challenges associated with modern semiconductor devices and ensuring their continued performance and reliability.

Table 3: Generalized comparison of thermal management types. (2 column, no color). **(Moore, & Shi, 2014).**

Thermal Management	Type	Cost	Ease of Installation	Performance
System-Level	Passive	1	1	2
	Active	2	2	3
Micro-Scale	Passive	4	4	4
Ratings (1= Low/Easy 5 = High/Hard)	Active	5	5	5

Microscale thermal management tech.s exhibit versatility, falling into either passive or active categories. Passive tech.s include microchannels, which effectively reduce thermal resistance by maximizing surface area directly for thermal conduction. Also, these microchannels can be micromachined directly into the bulk semiconductor or even other materials. Additionally, they can serve as "microtubes," facilitating the wicking of coolant closer to on-chip hotspots through surface tension**. (Martinez et al., 2016).** The passive dissipation of heat from great heat flux areas is achieved through the evaporation along with re-condensation of the coolant.

On the other hand, micro-scale active cooling devices leverage miniaturized refrigeration or cooling systems, often based on thermoelectric devices. These devices convert electricity right into heat directly for cooling/warming utilisations **(Martinez et al., 2016).** They operate on either the Peltier or even Stirling refrigeration cycle, with Stirling cycle devices generally outperforming Peltier cycle devices. Despite their higher performance, micro-refrigerators, being active chip-level devices, necessitate electrical connections for operation. A generalized contrast of these discussed MTM types is provided in Table 4, offering insights into their characteristics and applications.

The semiconductor industry has witnessed a proliferation of advanced packaging tech.s to accommodate the diverse needs of housing semiconductors. These advanced packaging tech.s include:

1. 2D Fan-Out (Chip-First) IC Integration
2. 2D Flip Chip IC Integration
3. Package-on-Package (PoP)
4. System-in-Package (SiP) or Heterogeneous Integration
5. 2D Fan-Out (Chip-Last) IC Integration
6. 2.1D Flip Chip IC Integration
7. 2.1D Flip Chip IC Integration with Bridges
8. 2.1D Fan-Out IC Integration with Bridges
9. 2.3D Fan-Out (Chip-First) IC Integration
10. 2.3D Flip Chip IC Integration
11. 2.3D Fan-Out (Chip-Last) IC Integration
12. 2.5D (Solder Bump) IC Integration
13. 2.5D (µBump) IC Integration
14. µBump 3D IC Integration
15. µBump Chiplets 3D IC Integration
16. Bumpless 3D IC Integration
17. Bumpless Chiplets 3D IC Integration

Their performance along with density ranges are visually represented in Fig. 2. Figure 3 illustrates advanced packaging tech.s' distinct groups, showcasing the breadth and diversity of options available for semiconductor integ. These packaging tech.s play a pivotal role in meeting the increasing demands for performance, miniaturization, and efficiency in the semiconductor industry.

GROUPS OF ADVANCED PACKAGING

A straightforward packaging method involves directly affixing the semiconductor chip onto a PCB, utilising methods like COB or DCA. Common packaging options include lead-frame packages like PQFP along with SOIC **(Abrams et al., 2020; Dai, 2016)**. According to **Zhu et al. (2020)**, both PBGA and fcCSP are considered typical packaging options for single chips. The definition of advanced packaging, as stated by **Tu et al. (2021)**, encompasses the integ. of 2D ICs with many chips on a package substrate, which is considered the basic need. The presence of a thin film layer upon the build-up package substrate (BuPS) classifies it as a 2.1D IC integ. with bridges. 2.3D IC integ. refers to the process of supporting multichips using a coreless inorganic or even organic TSV-less interposer along with attaching them to a BuPS. 2.5D IC integ. refers to the attachment of multichips on a PS using a passive TSV-interposer. 3D IC integ. refers to the attachment of multichips on a PS using an active TSV-interposer.

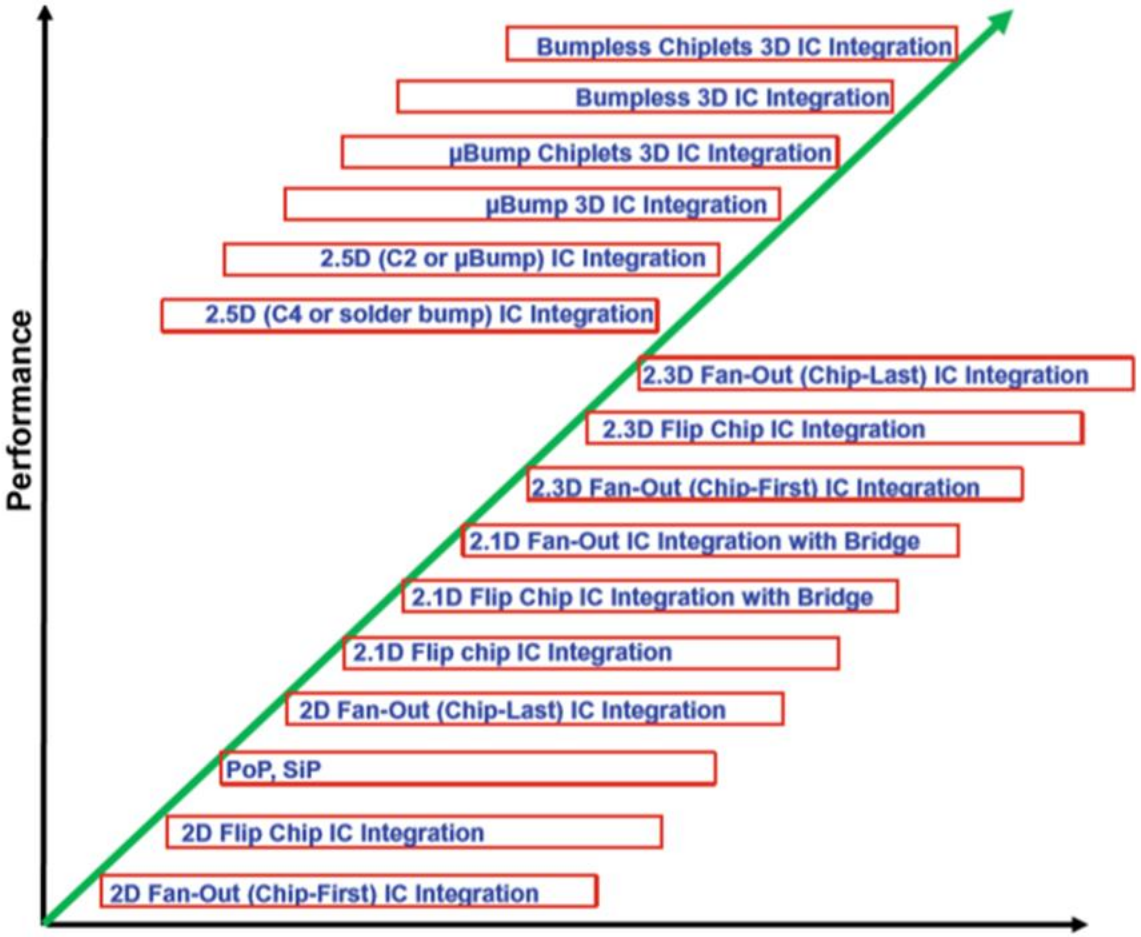

Figure 3: Density and performance ranges of advanced packing (Lau et al 2021)

2D FAN-OUT (CHIP-FIRST) IC INTEGRATION

Figure 4 illustrates a case study **(Chai, et al 2021)** of 2D fan-out utilising chip-first (die face-down) IC integ. **(Ezhilarasu, et al 2020)**. A total of four chips that are initially inserted in an EMC and subsequently expanded with RDLs, before being attached to solder balls. The solder balls are affixed to it directly. **(Bhutani, et al 2021)**.

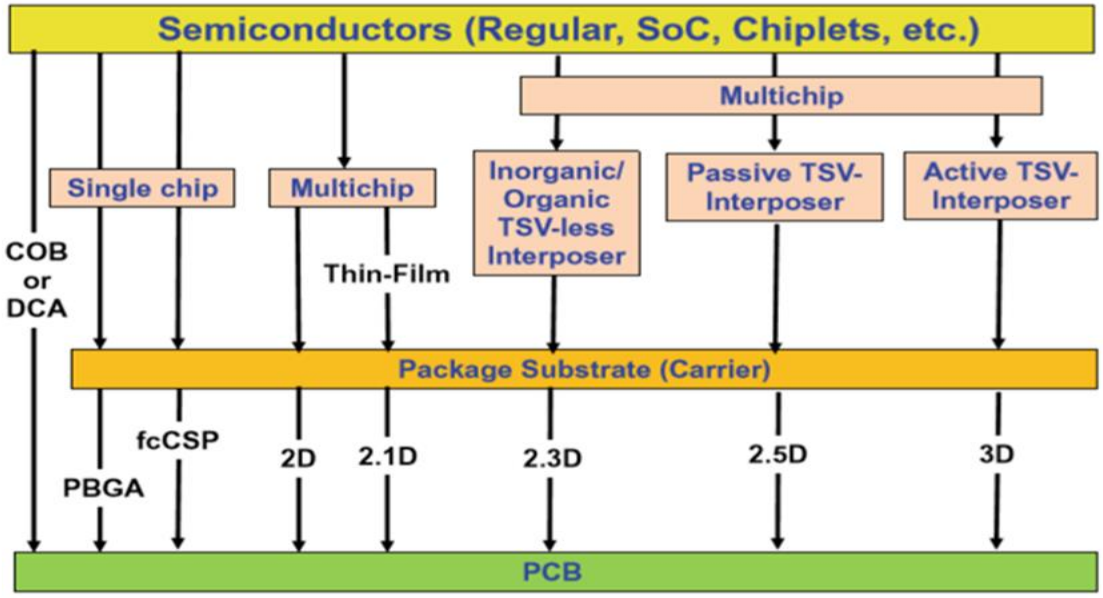

Figure 4: Advanced packing 2D,2.ID,2,5D, and 3D IC integration (Lau, et al 2021)

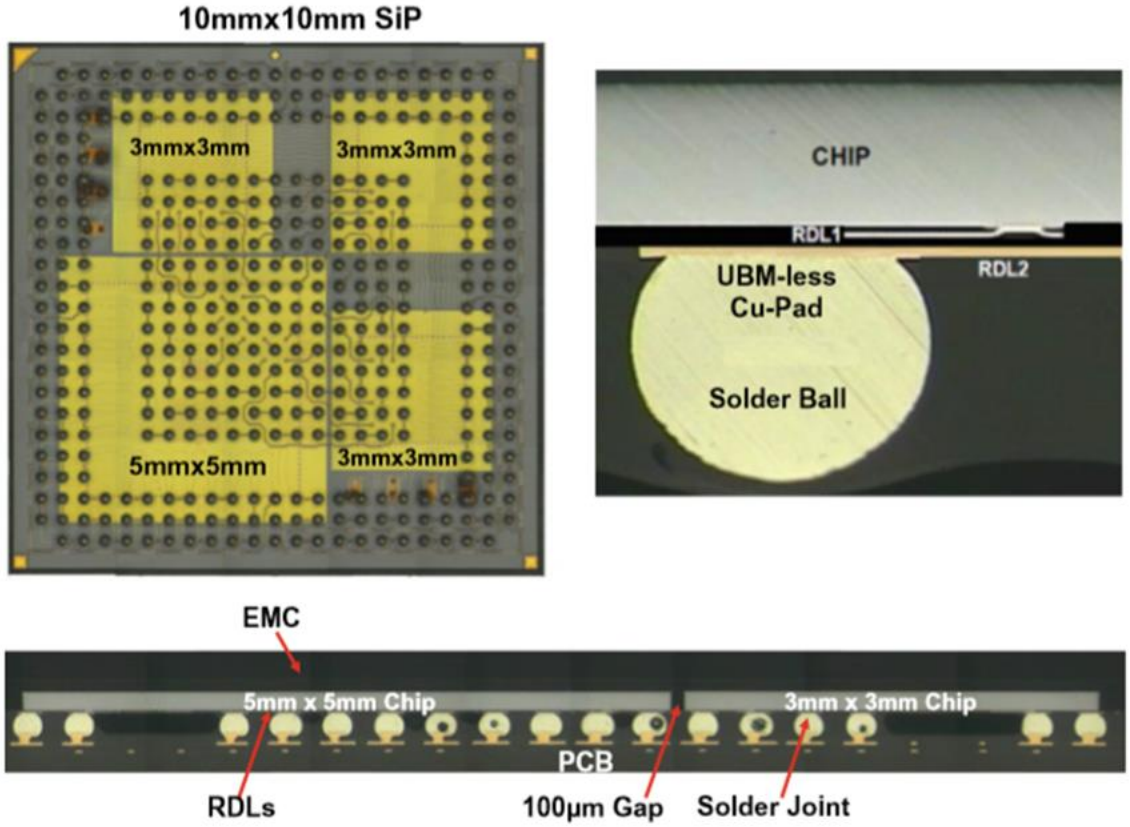

Figure 5: 2D fan out with chip first of 4 chips IC integration (Lau, et al 2021)

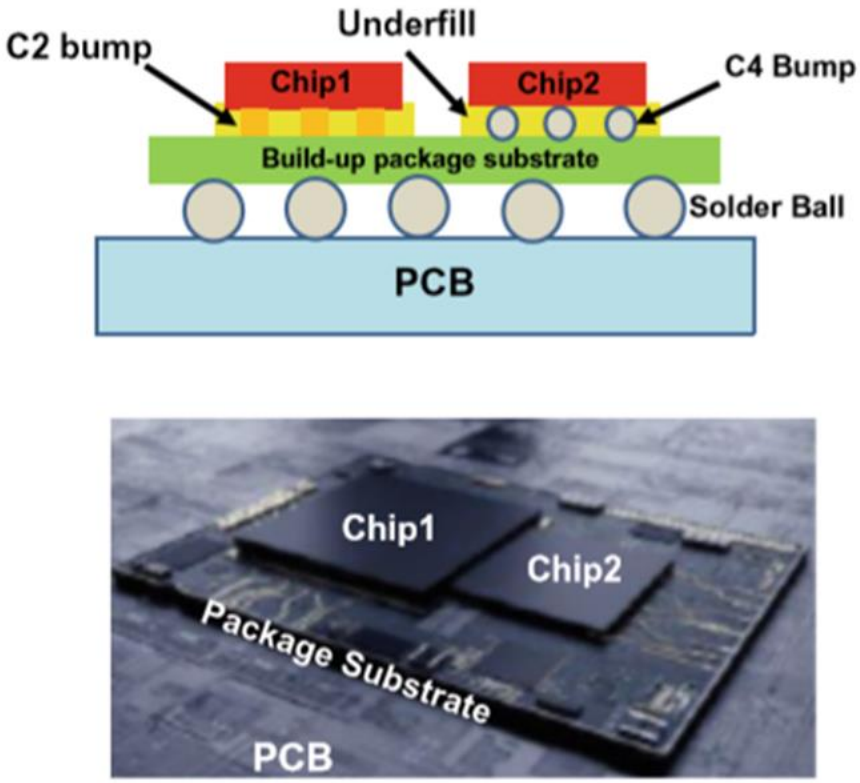

Figure 6: 2D flip chip IC intergration (Lau, et al 2021)

2D Flip Chip IC Integration

Figure 6 depicts a demonstration of 2D flip chip integrated circuit integ. The chips are fastened to a BuPS utilizing either C4 bumps or C2 bumps. Typically, there is a requirement for underfill material to be present across the chips along with the PS. Next, the PS is affixed to the PCB **(Seok, *et al*, 2020)**

PoP, SiP, and Heterogeneous Integration

Figure 7 depicts a demonstration of PoP on a Samsung smartwatch. The lower package accommodates both the applied processor (AP) along with the PMIC in close proximity, employing a fan-out along with chip-first manufacturing process, **(Wesling, 2020).**

The upper package lodges the controller, DRAM along with NAND, which is a Boolean operator along with logic gate.

Figure 8 depicts an illustration of a SiP utilized in an Apple smartwatch. It is evident that all the chips and discrete components (system) are integrated onto a single PS (package).

Figure 9 depicts an instance of heterogeneous integ. right for the IBM 9121 TCM. The ceramic substrate contains a total of 121 chips, each measuring approximately 8-10 square millimeters. The substrate consists of 63 layers. Also, the thermal performance is excellent, with a maximum dissipation of 10 W per chip along with 600 W per TCM.

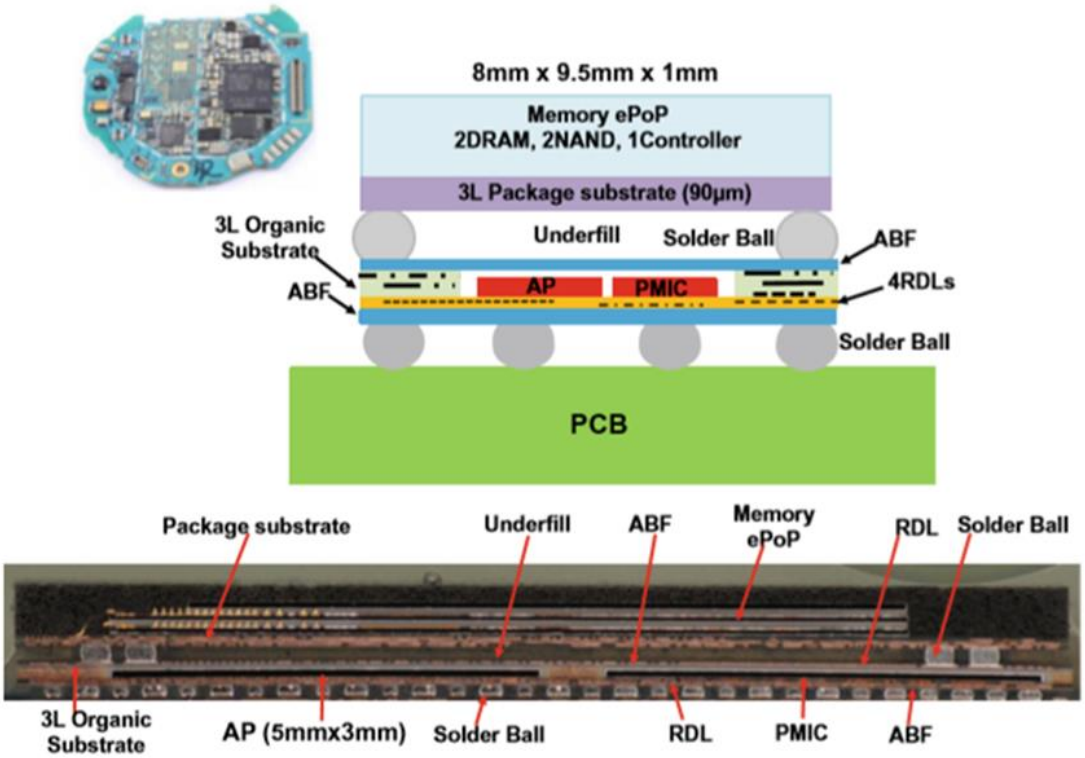

Figure 7: PoP with 2D fan out (chip first) IC integration in the bottom package (Wesling 2020)

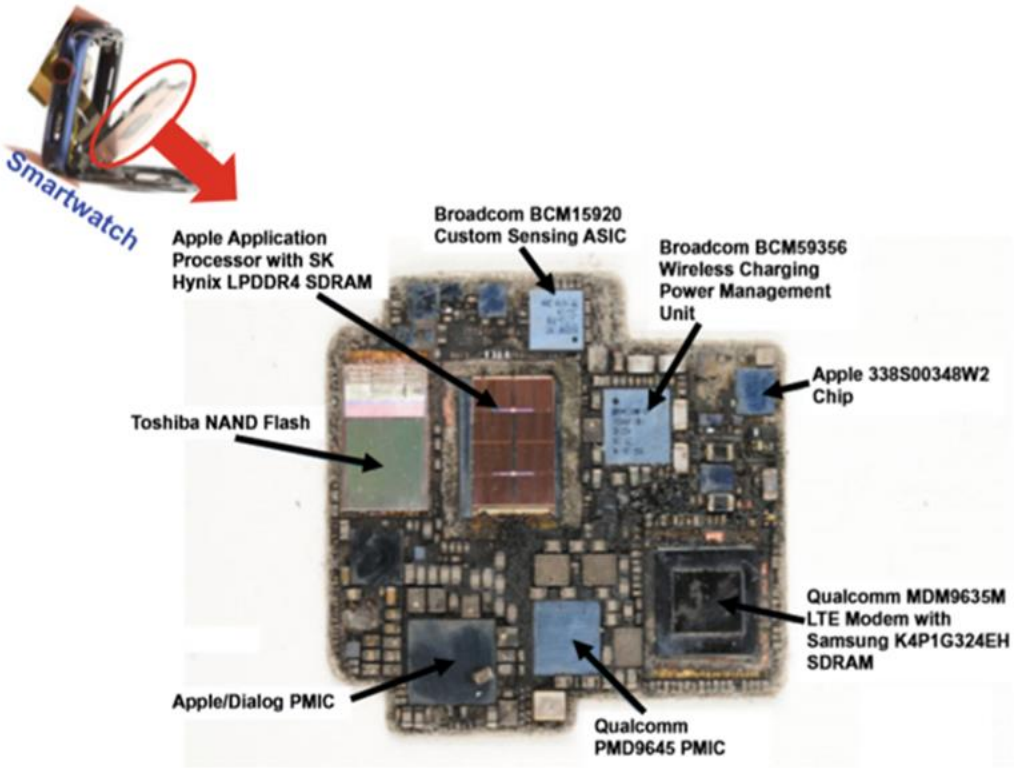

Figure 8: SiP with 2D IC integration (Sun & Wong 2019)

IBM 9121 TCM (Thermal Conduction Module)

- TCM weighs 2.2Kg
- Contains up to 121 chips about 8-10mm square
- Each chip has a spring-loaded Cu piston to remove heat
- Up to 10W dissipation per chip
- Up to 600W dissipation per TCM

  Ceramic substrate has:
  - 63 layers
  - Up to 400m of wirings
  - Up to 2 million vias
- 5Kg air-cooled heatsink to remove heat from TCM

Figure 9: Heterogeneous integration of 2D (of 121 chips) IC integration on ceramic subtrate

2D Fan-Out (Chip-Last) IC Integration

Figure 10 illustrates an instance of fan-out in chip-last IC integ., as demonstrated by Chai et al. in 2021. The initial fabrication process involves creating fan-out RDLs along with a metal line width along with spacing (L/S) of 2/2µm. Next, the process involves bonding chips to the RDL-substrate using microbump tech., which consists of a copper pillar and solder cap. Additionally, the RDL-substrate is stuck to the PCB using solder balls. The SEM image displays many components, including chips, along with microbumps, along with RDL-substrate, along with solder joints, along with PCB.

2.1D Flip Chip IC Integration

Figure 11 depicts a demonstration of 2.1D flip chip integrated circuit integ. Thin-film layers are visibly constructed on the surface of the BuPS. The metal line/space (L/S) dimensions of the thin-film layers can be reduced to a minimum of 2/2µm, enabling the use of flip chips incorporating microbumps (**Koh, 2020).**

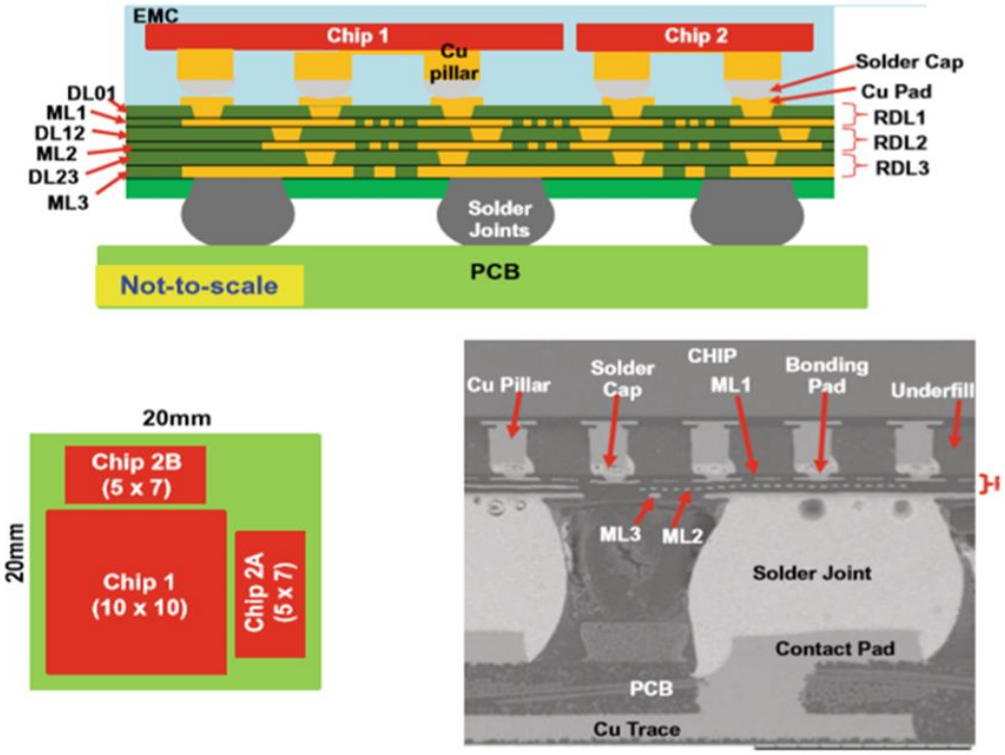

Figure 10: 2D fan out with chip last of three chips IC integration (Koh 2020)

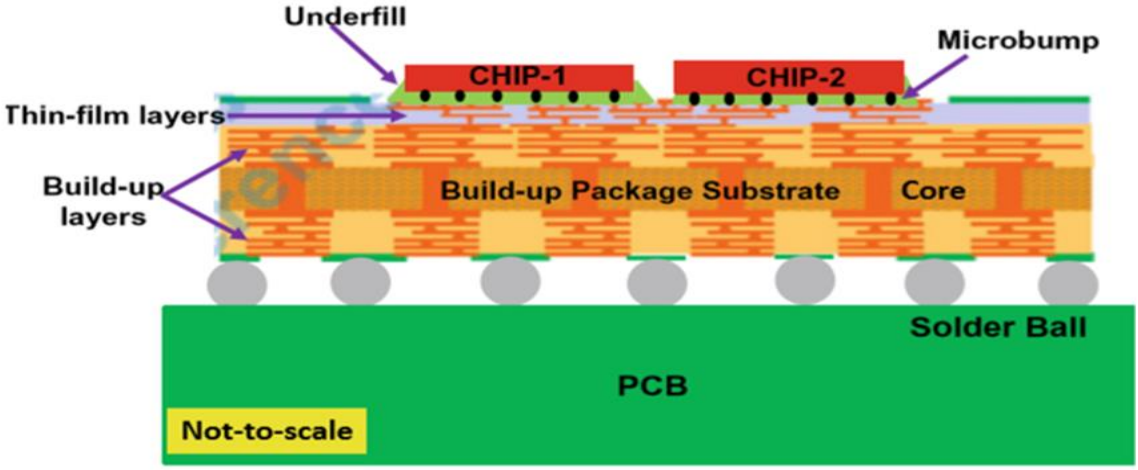

Figure 11: ID flip chip Ic integration(Koh 2020)

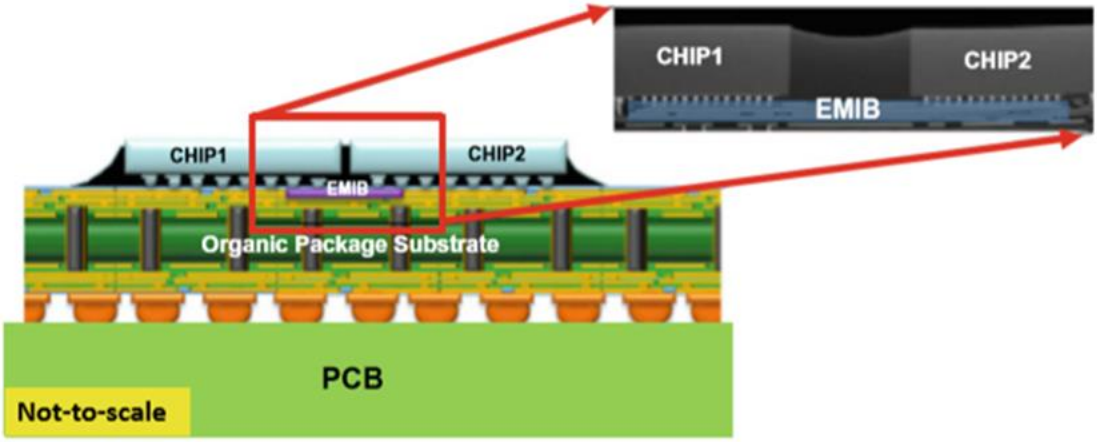

Figure 12: ID flip chip IC intergration with bridge (Jang et al 2021)

2.1D Flip Chip IC Integration with Bridges

Figure 12 depicts a case of 2.1D flip chip integrated circuit (IC) assembly, where Intel has supplied the bridges **(Duan, et al 2021)**. The EMIB, or embedded multi-die interconnect bridge, is integrated into the upper layer of a BuPS. Its purpose is to provide lateral communication between the two flip chips. Also, this packaging tech. is designed to supplant the TSV (via silicon via)-interposer tech.

Figure 13 illustrates an instance of 2.1D fan-out IC integ. with bridges, as demonstrated by Applied Materials **(Ko, et al 2020)**. To obtain further details on this topic, please refer to the provided source. The bridge is visibly encased within an EMC, rather than being housed in a BuPS. To obtain additional details regarding the integ. of fan-out ICs with bridges in a 2.1D configuration, please refer to the following material.

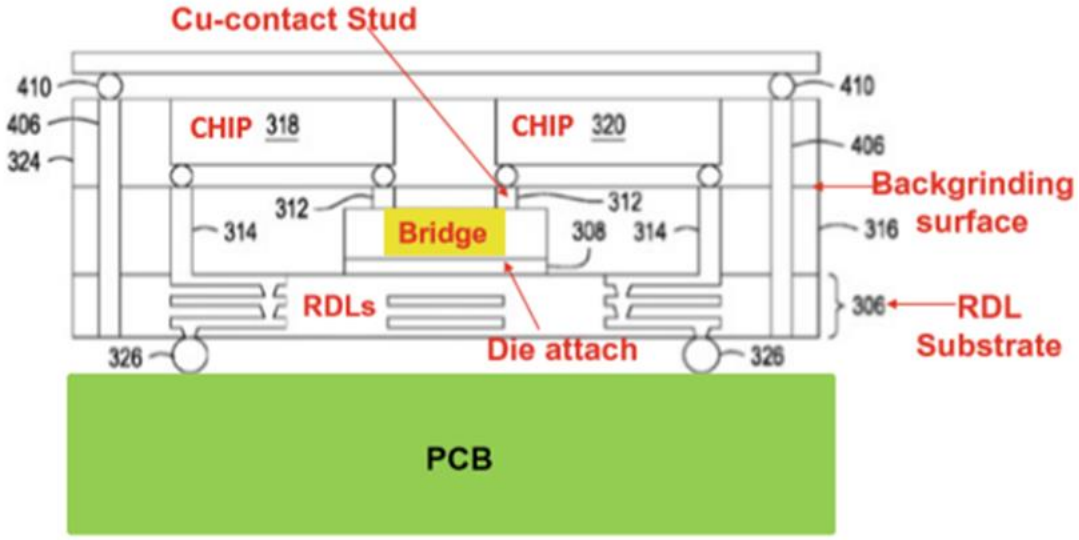

Figure 13: ID fan out IC intergration with bridge (Ko et al 2020)

2.3D Flip Chip IC Integration

Figure 14 is a demonstration of 2.3D flip chip integrated circuit integ. as demonstrated by Cisco **(Thadesar, & Bakir, 2019)**. The coreless organic substrate, also known as an interposer, is positioned over a BuPS and provides support for a SoC and several HBMs. To obtain additional details regarding the integ. of 2.3D flip chip ICs, please refer to the provided material.

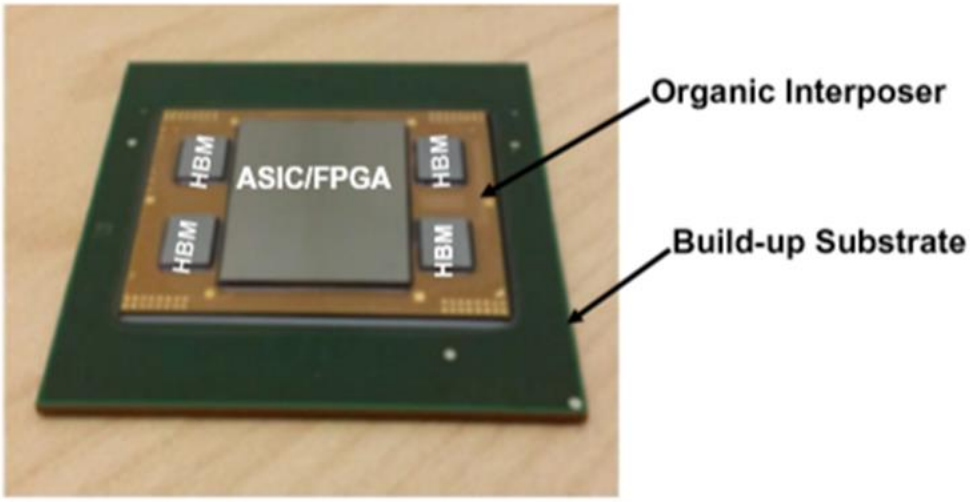

Figure 14: 2.3D flip chip IC integration (Thadesar, & Bakir 2019)

2.5D (C4 Bump) IC Integration

RF chip along with the logic chip are soldered onto the passive TSV-interposers (silicon carriers 1 along with 2) using C4 solder bumps. To obtain further details regarding the integ. of 2.5D (C4 bump) ICs, please refer to the provided material.

2.5D (C2 Bump) IC Integration

The GPU along with the HBM 2 are connected using C2 μ bumps on the passive TSV-interposer. Subsequently, the entire module is affixed to a packaging substrate utilizing C4 bumps. (**Park et al. 2021).**

Industry and Market Trends

The communications era is undergoing a transformative phase marked by a surge in innovative product introductions, including 2G, along with 2.5G, along with 3G cellular phones, along with PDAs, along with Digital Still Cameras, along with Digital Camcorders, along with PDA Cameras, along with Bluetooth-enabled products, along with Internet Audio Players. Consumer electronics applications, witnessing a five-year CAGR of 16%, are projected to surpass $45 million in 2005. The growth trajectory is primarily driven by Video games and Digital TV.

Key Drivers and Challenges:

- The demand for cellular phones remains robust, with an estimated shipment of approximately 600 million phones in 2005. Smartphones, expected to reach close to 200 million units in 2007, play a pivotal role in this growth.
- Consumers increasingly rely on their handsets for diverse functionalities such as listening to music, capturing and sharing photos, recording and watching videos, gaming, organizing activities, and accessing the Internet, contributing to the surge in system memory necessities and the requirement for SiP solutions.
- Challenges arise with complex SoC products' introduction incorporating RF along with Analog integ. across digital cores. Leading-edge semiconductor companies utilize Advanced CMOS tech. along with Mixed Signal High Voltage Technology for optimizing SoC, considering cost-performance benefits.
- The adoption of advanced CMOS silicon tech. with copper interconnect along with ultra-low-k dielectric materials is witnessing rapid growth, posing significant packaging development challenges, particularly beyond the 65nm CMOS process node (Shih, & Wong, 2021).

Design Considerations:

Product designers grapple with decisions on whether to design new products utilising SoC, along with SiP, or a combination of both. Functionality increases over time for both SiP and SoCs, with cost emerging as the decisive factor at any given time **(Shih, & Wong, 2021).**

Future Implications

The dynamic landscape outlined by these trends is poised to have a profound impact on packaging tech. necessities in the coming five years. The industry is expected to navigate evolving challenges while embracing advancements, setting the stage for continued innovation in communications and semiconductor packaging **(Shih, & Wong, 2021).**

CONCLUSION

In conclusion, the semiconductor industry is now poised for a revolution in the following five years, driven by key factors such as advanced CMOS tech. , scaling, increased integ., along with greater performance, along with thermal density demands. The growth in consumer electronics, along with mobile handsets, and automotive electronics further propels this transformation. The surge in device complexity will spark innovative and disruptive packaging solutions, fostering a diverse landscape in packaging tech.s. In certain markets, the choice of packaging tech. is anticipated to be a pivotal factor influencing purchasing decisions. The overarching challenge lies in developing cost-effective packaging solutions that align with the silicon cost reduction learning curve, despite the myriad technological hurdles that must be overcome. The future of advanced packaging tech. in semiconductors promises to reshape the industry, marking a significant leap forward in meeting evolving demands and driving unparalleled innovation.

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